

FAIRCHILD MEMORIES

READ ONLY MEMORIES

BIPOLAR ROMs AND PROMs

Item	Organization	DEVICE NO.	Description ⁽¹⁾	Address Access Time ns (Typ)	Chip Select Access Time ns (Typ)	Read Cycle Time		Power Dissipation mW (Typ)	Logic/Connection Diagram	Package(s)
						0°C to +70°C ns (Max)	-55°C to +125°C ns (Max)			
TTL										
1	16x48x8	93458	FPLA,OC	25	15	—	—	750	M20	8E,9Y
2	16x48x8	93459	FPLA,3S	25	15	—	—	750	M20	8E,9Y
3	256x4	93457	ROM,OC	25	12	45	60	425	M17	3D,6D,9B
4	256x4	93467	ROM,3S	25	12	45	60	425	M17	3D,6D,9B
5	256x4	93417	PROM,OC	25	12	45	60	425	M17	3D,6D,9B
6	256x4	93427	PROM,3S	25	12	45	60	425	M17	3D,6D,9B
7	512x4	93436	PROM,OC	30	15	50	60	475	M10	3D,6D,9B
8	512x4	93446	PROM,3S	30	15	50	60	475	M10	3D,6D,9B
9	512x4	93431	ROM,OC	30	15	50	60	475	M10	4B,6D,9B
10	512x4	93441	ROM,3S	30	15	50	60	475	M10	4B,6D,9B
11	512x8	93432	ROM,OC	35	15	55	70	650	M11	4R,6M,7L,9N
12	512x8	93442	ROM,3S	35	15	55	70	650	M11	4R,6M,7L,9N
13	512x8	93438	PROM,OC	35	15	55	70	650	M11	4R,6M,7L,9N
14	512x8	93448	PROM,3S	35	15	55	70	650	M11	4R,6M,7L,9N
15	1024x4	93452	PROM,OC	30	15	55	70	650	M18	8F,9M
16	1024x4	93453	PROM,3S	30	15	55	70	650	M18	8F,9M
17	1024x8	93450	PROM,OC	30	20	45	60	550	M21	4R,6M,9N
18	1024x8	93451	PROM,3S	30	20	45	60	550	M21	4R,7L,9N
19	1024x8	93454	ROM,OC	30	20	45	60	550	M12	4R,6M,7L,9N
20	1024x8	93464	ROM,3S	30	20	45	60	550	M12	4R,6M,7L,9N

ECL

21	256x4	10416	PROM	15	4.0	25 ⁽²⁾	—	650	M19	4B,6D
22	256x4	100416	PROM	15	4.0	25 ⁽²⁾	—	650	M19	4B,6D

1. OC = open collector, 3S = 3-state

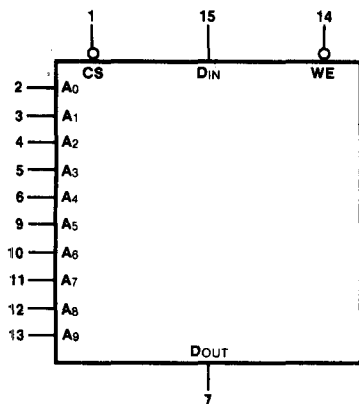
2. -30°C to +85°C

10

MEMORY

M6

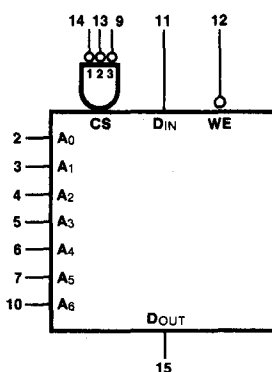
93415, 93L415, 93415A,
93425, 93L425, 93425A



V_{CC} = Pin 16
GND = Pin 8

M7

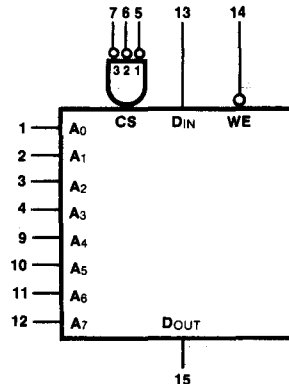
10405



V_{CC} = GND = Pins 1 and 16
V_{EE} = Pin 8

M8

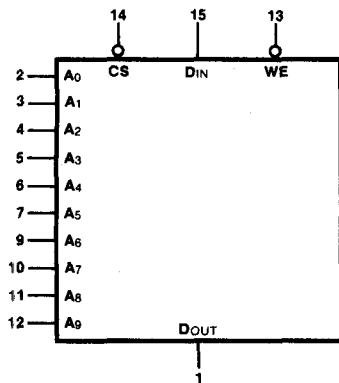
10410, 10411, 10414
100414



V_{CC} = Pin 16
V_{EE} = Pin 8

M9

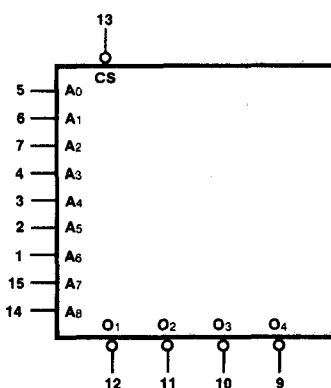
10415, 10415A, 100415



V_{CC} = Pin 16
V_{EE} = Pin 8

M10

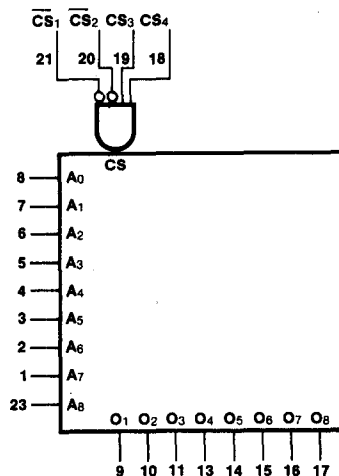
93431, 93441
93436, 93446



V_{CC} = Pin 16
V_{EE} = Pin 8

M11

93432, 93442
93438, 93448



V_{CC} = Pin 24
GND = Pin 12