MOS
LSI

TMS 40L45 JL, NL; TMS 40L47 JL, NL
1024-WORD BY 4-BIT STATIC RAMs

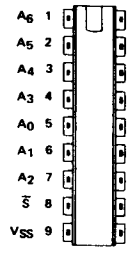
NOVEMBER 1977

- 1024 x 4 Organization
- Single 10% Tolerance 5-V Supply
- High Density 300-mil 18- and 20-Pin Packages
- Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)
- 3 Performance Ranges:

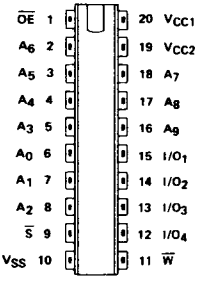
	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 40L45-25, TMS 40L47-25	250 ns	250 ns
TMS 40L45-30, TMS 40L47-30	300 ns	300 ns
TMS 40L45-45, TMS 40L47-45	450 ns	450 ns

- 400-mV Guaranteed Noise Immunity With Standard TTL Loads – No Pull-Up Resistors Required
- Common I/O With Three-State Outputs and Chip Select Control for OR-Tie Capability
- Fan-Out to 1 Series 74 or 74S TTL Load – No Pull-Up Resistors Required
- Low Power Dissipation
  - 250 mW *Typical
  - 370 mW *Maximum
- Standby Power Dissipation (TMS 40L47)
  - 12 mW Typical
  - 24 mW Maximum

TMS 40L45
18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



TMS 40L47
20-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



PIN NAMES	
A_0-A_9	Addresses
I/O_1-I/O_4	Data input/output
$\overline{OE}$	Output Enable
$\overline{S}$	Chip Select
V_{CC} (TMS 40L45)	+5-V Supply
V_{CC1} (TMS 40L47)	+5-V Supply (array only)
V_{CC2} (TMS 40L47)	+5-V Supply (periphery only)
V_{SS}	Ground
$\overline{W}$	Write Enable

description

This series of low power static random-access memories is organized as 1024 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Series 74 or 74S TTL. No pull-up resistors are required. The TMS 40L45/40L47 series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. Both the TMS 40L45 and 40L47 are characterized to retain data at V_{CC} = 2.4 V to reduce power dissipation. Furthermore for applications such as battery backup, the TMS 40L47 has separate V_{CC} pins for the array and periphery, and data will be retained if power solely to the array is maintained.

*5% supply tolerance

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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TMS 40L45 JL, NL; TMS 40L47 JL, NL
1024-WORD BY 4-BIT STATIC RAMs

he TMS 40L45 series and the TMS 40L47 series are offered in 18-pin and 20-pin respectively dual-in-line ceramic (JL uffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. The series is esigned for operation from 0°C to 70°C.

ion

ddresses (A0-A9)

he ten address inputs select one of the 1024 4-bit words stored in the RAM. The address-inputs must be stable for the uration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external ull-up resistors.

utput enable ($\overline{OE}$)

he output enable terminal, which can be driven directly from standard TTL circuits, affects only the data-in/data-out erminals. When output enable is at a logic high level, the I/O terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

hip select ($\overline{S}$)

he chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in/data-out erminals. When chip select and output enable are at a logic low level, the I/O terminals are enabled. When chip select is igh, the I/O terminals are in the floating or high-impedance state and the input is inhibited.

rite enable ($\overline{W}$)

he read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low elects the write mode. $\overline{W}$ must be high when changing addresses to prevent erroneously writing data into a memory ocation. The $\overline{W}$ input can be driven directly from standard TTL circuits.

ata-in/data-out (I/O_1-I/O_4)

Data can be written into a selected device when the write enable input is low. The I/O terminal can be driven directly rom standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fan-out of one Series 74 TTL gate or one Series 74S TTL gate. The I/O terminals are in the high impedance state when chip select ($\overline{S}$) s high or whenever a write operation is being performed. Data-out is the same polarity as data-in.

ıy operation

There are two basic standby modes available to retain data when operating the TMS 40L45/40L47 series:

1. Reduce the V_{CC} supply to 2.4 V
2. Supply power to the array only (TMS 40L47 only).

Combining 1 and 2 on the TMS 40L47 will produce the lowest possible standby power while retaining data.

DEVICE	SUPPLY	OPERATING	STANDBY	
TMS 40L45	V_{CC}	+5 V	+2.4 V	
TMS 40L47	V_{CC1}	+5 V	+5 V	+2.4 V
	V_{CC2}	+5 V	0 V	0 V

(nominal supply values)

During standby operation, data cannot be read or written into the memory. When resuming normal operation, five cycle times must be allowed after normal supplies are returned for the memory to resume steady-state operating conditions.

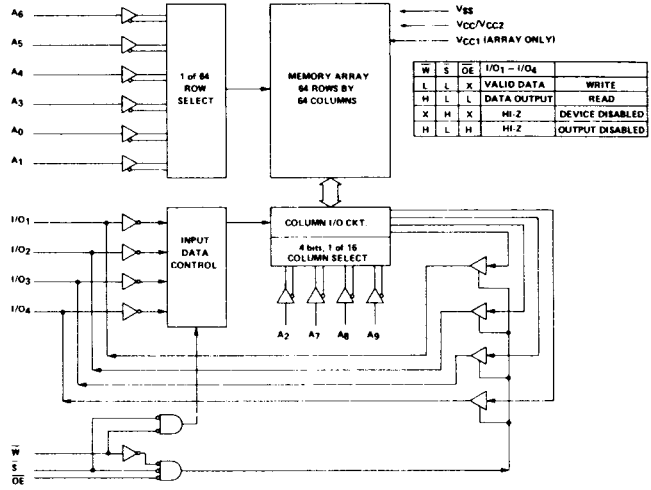
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.5 to 7 V
Input voltage (any input) (see Note 1)	−0.5 to 7 V
Continuous power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

functional block diagram



W	S	OE	I/O1 – I/O4	
L	L	X	VALID DATA	WRITE
H	L	L	DATA OUTPUT	READ
X	H	X	HI-Z	DEVICE DISABLED
H	L	H	HI-Z	OUTPUT DISABLED

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (TMS 40L45)	Operating	4.5	5	5.5	V
	Standby	2.4	5	5.5	
Supply voltage (array only), V_{CC1} (TMS 40L47)	Operating	4.5	5	5.5	V
	Standby	2.4	5	5.5	
Supply voltage (periphery only), V_{CC2} (TMS 40L47)	Operating	4.5	5	5.5	V
	Standby	0	0	5.5	
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}		2		5.5	V
Low-level input voltage, V_{IL}		−0.3		0.8	V
Operating free-air temperature, T_A		0		70	C

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Electrical characteristics over recommended operating free air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High level voltage	I_{OH} = −200 μA	V_{CC} = 4.75 V	2.4			V
			V_{CC} = 4.5 V	2.2			
V_{IL}	Low level voltage	I_{OL} = 2 mA	V_{CC} = 4.5 V			0.4	V
I_I	Input current	V_I = 0 V to 5.5 V				10	μA
I_{O2}	Off-state output current	$\overline{S}$ or $\overline{OE}$ at 2 V or $\overline{W}$ at 0.8 V	V_O = 0 to 5.5 V			10	μA
I_{CC}	Supply current from V_{CC}	I_O = 0 mA, T_A = 0°C (worst case)	V_{CC} = 5.5 V		55	70	mA
			V_{CC} = 2.4 V		40	50	
I_{CC1}	Supply current from V_{CC1} (array only)	I_O = 0 mA, T_A = 70°C (worst case)	V_{CC} = 5.5 V		5	20	mA
			V_{CC} = 2.4 V		5	10	
I_{CC2}	Supply current from V_{CC2} (periphery only)	I_O = 0 mA, T_A = 0°C (worst case)	V_{CC} = 5.5 V,		50	70	mA
C_i	Input capacitance	V_I = 0 V,	f = 1 MHz			8	pF
C_o	Output capacitance	V_O = 0 V,	f = 1 MHz			12	pF

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

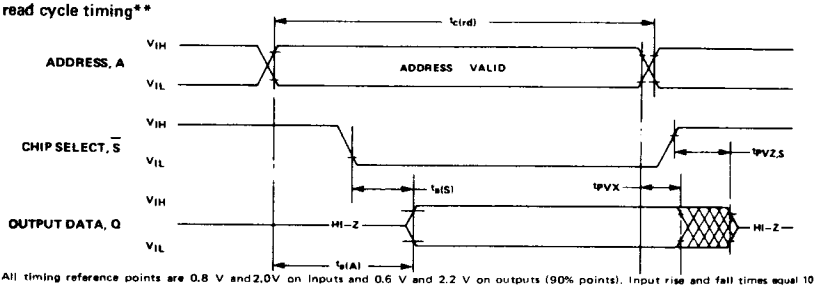
Timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	TMS 40L45-25 TMS 40L47-25		TMS 40L45-30 TMS 40L47-30		TMS 40L45-45 TMS 40L47-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	250		300		450		ns
$t_{c(wr)}$	Write cycle time	250		300		450		ns
$t_{w(W)}$	Write pulse width	100		150		200		ns
$t_{su(A)}$	Address set up time	0		0		0		ns
$t_{su(S)}$	Chip select set up time	100		150		200		ns
$t_{su(D)}$	Data set up time	100		150		200		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{h(A)}$	Address hold time	20		20		20		ns
$t_{t(A)}$	Address transition time	5	200	5	200	5	200	ns

switching characteristics over recommended voltage range, T_A = 0°C to 70°C, 1 series 74 TTL load, C_L = 100 pF

PARAMETER		TMS 40L45-25 TMS 40L47-25			TMS 40L45-30 TMS 40L47-30			TMS 40L45-45 TMS 40L47-45			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
$t_{a(A)}$	Access time from address			200			300			450	ns
$t_{a(S)}$	Access time from chip select (or output enable) low			100			100			120	ns
$t_{a(W)}$	Access time from write enable high			100			100			120	ns
t_{PVX}	Output data valid after address change	10			10			10			ns
$t_{PVZ,S}$	Output disable time after chip select (or output enable) high			40			80			100	ns
$t_{PVZ,W}$	Output disable time after write enable high			40			80			100	ns

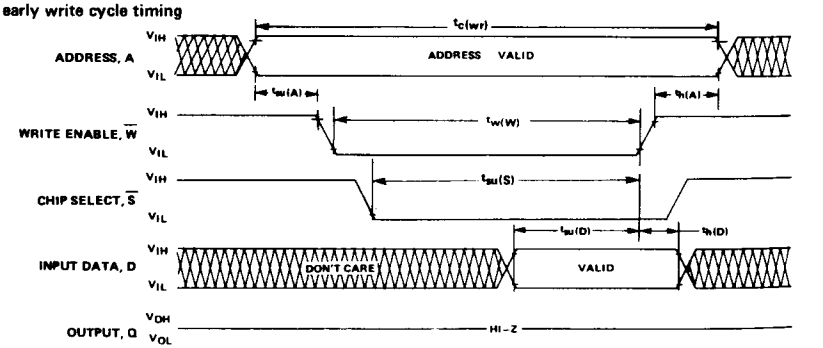
read cycle timing**



All timing reference points are 0.8 V and 2.0V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times equal 10 nanoseconds.

**Write enable is high for a read cycle.

early write cycle timing



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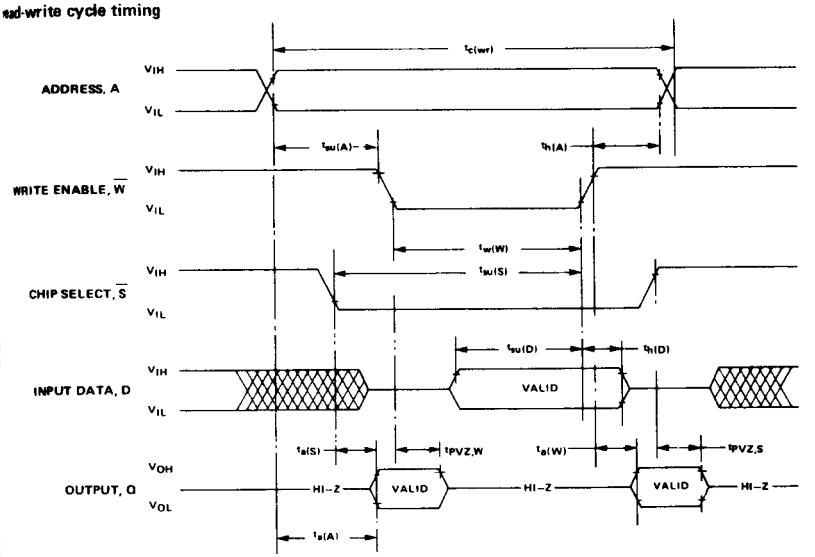
ead-write cycle timing



pplications data

Early write cycle avoids I/O conflicts by controlling the write time with $\overline{S}$. In the diagram above, the write operation will be controlled by the leading edge of $\overline{S}$, not $\overline{W}$. Data can only be written when both $\overline{S}$ and $\overline{W}$ are low. Either $\overline{S}$ or $\overline{W}$ being high inhibits the write operation and data stored will not be affected by the address. To prevent erroneous data being written into the array, the addresses must be stable during the write cycle as defined by $t_{su(A)}$, $t_w(W)$, and $t_{h(A)}$.