Application Note AN1116

Introduction to Cypress SRAMs - AN1116

Abstract

An SRAM is a memory element that is a key part of the core of many systems. Most high-performance systems have SRAMs in them. SRAM stands for Static Random Access Memory. SRAMs differ in many respects from other kinds of memories. The difference comes from the implementation of the memory structure in SRAMs. This application note is intended to give a first time reader an introduction to SRAM basics and the different kinds of SRAMs. It is not intended to be a design guide on SRAMs

SRAMs – An Introduction

Most systems contain the following kinds of memories:

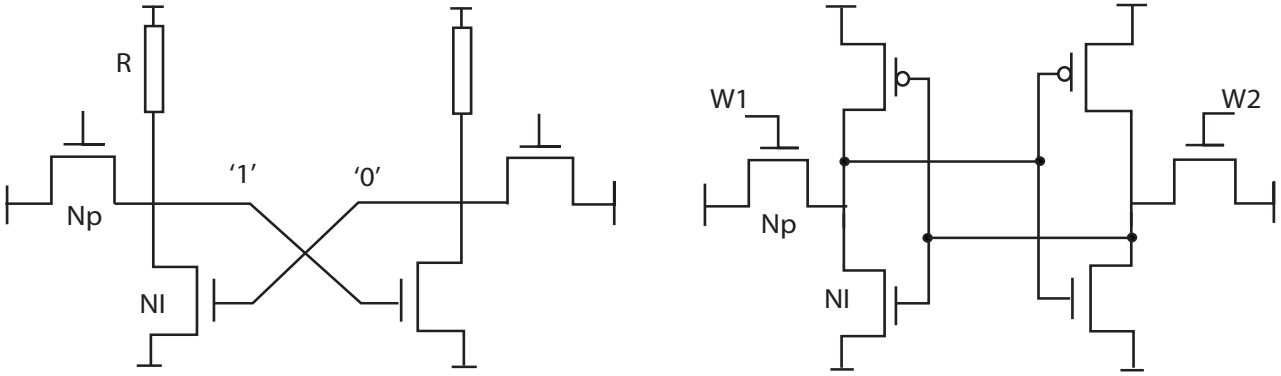
- PROM
- EPROM
- EEPROM/Flash
- DRAM
- SRAM

PROMs, EPROMs, and Flash memories come under the category of nonvolatile memories. Nonvolatile memories are devices that will store data even when the power to the device is removed. PROMs, EPROMs, and Flash memories differ in the technology used and method by which the user reprograms the device and the method by which the user erases the data in the memory device.

SRAM and DRAM are random access memories, that can store data as long as power is applied to the device. If the power is ever removed, all data that was stored in the memory will be lost. Even when powered, in DRAMs data could be lost if it is not periodically refreshed; while in SRAMs the data can be stored without any kind of extra processing or refreshing. The data will remain in the SRAM once it has been written there, as long as the power supply to the device is maintained.

SRAMs are differentiated from their other memory counterparts by the type of the memory cell. Nearly all SRAMs either use a 4-transistor or a 6-transistor Memory Cell. These cell structures allow data to be stored for an indefinite amount of time in the device as long as it is powered. Figure 1 below shows the 4-transistor and the 6-transistor cell. (These are usually referred to as the 4-T and the 6-T cells, respectively.) The SRAM cell is formed by two cross-coupled inverters. System evolution over time has led to the creation of different types of SRAMs. The next section goes into the details of the different kinds of SRAMs and their applications.

Figure 1. The 4-T and the 6-T Memory Cells



4 Transistor Memory Cell (4T Cell)

6 Transistor Memory Cell (6T Cell)

Types of SRAM

SRAMs basically come in two different flavors: synchronous and asynchronous.

Synchronous SRAMs are devices that are synchronized with an external signal called a clock. The device will read and write information into the memory only on particular states of the clock. The particular state of interest is when the clock switches, i.e., when it goes from either LOW-to-HIGH ("rising edge"), or from HIGH-to-LOW ("falling edge").

An asynchronous SRAM, on the other hand, does not depend on the state of a clock. It will begin to read or write information into the memory as soon as it receives the instruction to do so.

Because asynchronous devices are slightly easier to understand, we will look at them first. These devices are typically subdivided into two different categories, based on their access time, which is the total time it takes for the device to output data after receiving a read instruction.

Asynchronous SRAM

a) Fast Asynchronous SRAMs

These are devices that typically operate in the sub–25 ns region. They are often used in buffer memory applications, Tag RAM for PC caches, etc.

Fast asynchronous SRAMs have been used for a long time and the market for these devices has matured to a stable level. The density range for these types of SRAMs is from the sub 4K to 32 Mb and have data words that are mostly configured as x1, x4, x8, x16 or x32. (This is the size in bits that each memory location can store.)

b) Slow Asynchronous SRAMs

These are devices that typically operate in the 45-ns and slower speed range. These SRAMs are typically designed to consume very low power and are used in applications where power is a major concern. Applications for these SRAMs include cellular phones, PDAs, radios, and pagers. In these applications, these devices are used for temporary data storage, as well as scratch pad applications.

Although slow SRAMs have also been around for several years, the recent surge in cell phone sales have expanded the market for these devices.

The density range for these SRAMs is usually from 256K to 16 Mb and are mostly configured with word widths of 8, 16 and 32 bits.

Synchronous SRAMs

The fastest growing segment of SRAMs is Synchronous SRAMs. Synchronous SRAMs come in many flavors. As was mentioned earlier, these devices are synchronized with an external clock. Unlike asynchronous devices, synchronous SRAMs have internal registers, which latch the inputs on every clock edge (either rising or falling) and, depending on the implementation, will sometimes have registers on the data output lines.

The following is a simplistic listing of the types of Synchronous SRAMs.

- Single Data Rate SRAMs
  - Pipelined vs. Flowthrough SRAMs
  - Burst SRAMs
  - Network SRAMs - NoBL™/ZBT™ SRAMs
- Double Data Rate SRAMs
  - Standard DDR SRAMs
  - QDR™ SRAMs
- NetRAM™

Single Data Rate Synchronous SRAMs

These are synchronous SRAMs where one word of data is transferred between the SRAMs and the controller in a given clock cycle.

SDR SRAMs differ in their implementations. Every implementation is optimized for the end application. Below are some various implementations for SDR SRAMs.

Pipelined vs. Flowthrough

All synchronous SRAMs have input registers, which will latch in the control signals, address, and data on the rising edge of the clock. An SRAM can also have output registers, which we will discuss briefly here.

A pipelined synchronous SRAM is one that has output registers. In other words, the output data will be clocked into a register before it is sent onto the data lines. It adds one clock cycle to the process of doing a read. For pipelined SRAMs, a write occurs in one clock cycle, while a read occurs in two.

A flowthrough SRAM, on the other hand, does not have output registers. Data that is sent out from the memory array is immediately placed on the external data lines. For a flowthrough synchronous SRAM, a write again takes one cycle, while a read will also take one cycle.

Burst SRAMs

These are SRAMs that were optimized for usage in PC cache applications. In many computer systems, it is beneficial to store as much data in the SRAM as possible so as to avoid multiple accesses. This becomes useful when several data words are accessed in a predefined sequence. A “burst” is an added feature that lets the memory use an internal counter to increment the address that was latched into the SRAM. Therefore, it is possible to retrieve up to four words of data from the memory on one command. Burst SRAMs can be pipelined or flowthrough. In either case, a burst SRAM will output data on every clock cycle. (A four-word burst will output data over 4 clock cycles.) The burst is activated by an input pin called “advance,” usually abbreviated ADV.

Network SRAMs — NoBL™/ZBT™ SRAMs

Another type of SDR SRAMs are networking SRAMs, or NoBL/ZBT SRAMs. NoBL stands for “No Bus Latency™” These SRAMs are designed for systems that require interleaved reads and writes. In regular synchronous SRAM (non-NoBL), a data hazard can occur when a write follows a read since write data would be placed on the bus on the same clock edge when the SRAM is trying to place the read data on the data lines. (For more on this, please refer to the application note AN1092 on bus contention.) An additional “wait state” would have to be added to allow the read to finish before executing the write. NoBL SRAMs allow such interleaved instructions without wasting any cycles. Eliminating these wait states makes NoBL SRAMs very attractive in networking applications, where maximum bus efficiency is extremely important.

Double Data Rate Synchronous SRAMs

These SRAMs are designed to be the SRAMs of choice for networking applications with high data rate requirements. QDR (Quad Data Rate™) and DDR (Double Data Rate) SRAMs belong to this family. These SRAMs can transfer multiple data words in a given cycle.

QDR SRAMs

QDR SRAMs are synchronous SRAMs with an innovative architecture designed especially for high-performance networking systems. These devices have two separate ports (for read and write operations) that can run independently at double data rate, i.e., up to two words can be written into the device and up to two words can be read from the device at the same time. The net result is four data items per clock cycle.

Much like NoBL SRAMs, applications such as ATM switches and routers will benefit from simultaneous reads and writes that can be done on the SRAM with no latency and the data through the SRAM is guaranteed even for simultaneous access to the same address location.

DDR SRAMs

DDR SRAMs are similar to QDR SRAMs except that these devices have only one port for both read and write operations, i.e., up to two words can be written into the device or up to two words can be read from the device at the same time.

These are generally used in very high performance (workstation and server) cache applications.

NetRAM™

NetRAM is another SRAM designed for networking applications. These devices allow concurrent reads and writes into the memory array. The device consists of a normal SRAM array with two ports each with independent address, data, and control buses. These SRAMs are useful in switching applications.

Conclusion

Cypress Semiconductor is one of the leading suppliers of Static Random Access Memories, and offers a broad selection of SRAMs to customers. As the need for high bandwidth increases due to high-performance networking and communication applications, Cypress has answered the call with some of the most intriguing technology in the SRAM market, including the revolutionary Quad Data Rate, NoBL and MoBL® SRAMs.

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