Apple Computer Schematics ... About Me

Here are a set of schematics for several computers and computer peripherals from Apple Computer.

Schematics were obtained from official Apple Computer micro-fische cards that originated from the Apple Computer factory in Carrollton Texas (just north of Dallas). These card images were scanned into digital TIFF graphic files.

Schematics cover the following:

Apple Lisa computer
Apple Macintosh computer
Apple II Monitor
Apple II Mouse
Apple ImageWriter Printer
Apple ProFile Hard Drive (5MB or 10MB)
Apple Widget Hard Drive (10MB)
Apple 3.5" 400K Micro-Floppy Disk Drive

Schematics were edited, renamed, and placed into folders by DTC for clarity sake (they were in a simple linear arrangement which was not very reader friendly). Schematic TIFF files were also converted to be in an uncompressed TIFF format so that they could be more quickly opened (the original compressed TIFF files have extension .TIF, the uncompressed files have extension .TIFF).

Each schematic was also saved as in PDF format for Adobe Acrobat Reader use. These PDF files should be the most portable and also print fully on whatever size paper you choose.

Catalogs of what appear in this set follow.

LISA Microfiche

Lisa/Mac128k/perpherials Microfiche

050-0074-C SCH SWEEP/PWR SUPPLY SHT 3-3 0044
050-0074-C SCH SWEEP/PWR SUPPLY SHT 2-3 0044
050-0074-C SCH SWEEP/PWR SUPPLY SHT 1-3 0044

630-0102-D ASSY PCH UNTSTD SWEEP/PWR SPLY 0244
630-0102-01-D ASSY PCH UNTSTD SWEEP/PWR SPLY 0244
050-0073-C SCHEMATIC, MAIN LOGIC BRD 3138

620-6179-A ASSY TOP 1/2 MB LISA 2/10 0244
620-5145-A SUBASSY DSK DR MODULE, LISA 2 0244
620-0140-A ASSY PROFILE CONTRLR, LISA-2.0 0044
620-5115-H SUBASSY VIDEO ONE LISA 3433
050-5028-C SCH.R/W BD, WIDGET SHT 1-4 3533
677-0140-C ASSY PCH UNTSTD READ/WRITE BD, WIDGET 3533
677-0103-C ASSY PCB UNTSTD MOTHER BD, WIDGET 3533
050-5028-C SCH.R/W BD, WIDGET SHT 3-4 3533
050-5028-C SCH.R/W BD, WIDGET SHT 4-4 3533
656-6121-A ASSY CHASSIS PROFILE-B SHT 1-3 3533
050-5028-C SCH.R/W BD, WIDGET SHT 2-4 3533
620-5130-A SUBASSY VIDEO ONE LISA 2.0 3493
620-5129-A SUBASSY CHASSIS TWO LISA 2.0 SHT 1-2 3493
620-5129-A SUBASSY CHASSIS TWO LISA 2.0 SHT 2-2 3493
620-5132-A SUBASSY CD CAGE LISA 2.0 3493
620-5128-A SUBASSY CHASSIS ONE-A LISA 2.0 3473

There are 2 of the following:
815-5032-A COUNTERWEIGHT ARM WIDGET 3413
815-5032-A COUNTERWEIGHT ARM WIDGET 3413

677-6000-A ASSY, HEAD/DISK WIDGET SHT 1-2 3413
677-6000-A ASSY, HEAD/DISK WIDGET SHT 2-2 3413
677-5016-A SUBASSY HEAD/DISK WIDGET SHT 1-2 3413
677-5016-A SUBASSY HEAD/DISK WIDGET SHT 2-2 3413
620-0142-D ASSY, PCB I/O BRD LISA-2.0 3363
677-5013-A SUBASSY ARM WIDGET SHT 2-2 3153
677-5013-A SUBASSY ARM WIDGET SHT 1-2 3153
050-5023-B SCH.MOTOR CONTROL WIDGET 3153
677-0103-B ASSY, PCH UNTSTED MOTHERBRD, WIDGET 3113
050-5024-B SCHEMATIC MOTHERBRD, WIDGET SHT 3-3 3113
050-5024-B SCHEMATIC MOTHERBRD, WIDGET SHT 2-3 3113
050-5024-B SCHEMATIC MOTHERBRD, WIDGET SHT 1-3 3113
620-5134-A SUBASSY CHASSIS THREE LISA, 2.0 0064
620-5133-A SUBASSY DSK DR 10 MB LISA 0064
620-5136-A SUBASSY BEZEL LISA, 2.0 0064
620-5135-A SUBASSY CHASSIS FOUR LISA, 2.0 0064
620-0019-L ASSY, PCB CPU BRD LISA 0104
590-0207-B CABLE ASSY MOTHERBD LISA CONTRLR SHT 1-2 0204
590-0207-B CABLE ASSY MOTHERBD LISA CONTRLR SHT 2-2 0204
590-0167-A ASSY INTERNAL CABLE 3 1/2" DR 0204
620-5203-L SUBASSY POWER SUPPLY LISA 2233
620-0119-J ASSY PCB CPU BD LISA 2233
620-0120-P ASSEMBLY PCB PWR SUPPLY BA 115V LISA 2233
620-5104-D SUBASSY CARD CAGE LISA 2233
620-8108-8 ASSY F/G LISA 2233
050-5006-E SCH. CONTRLR, PROFILE 3253
050-5005-H SCH ANALOG BD PROFILE 0244
050-5027-A SCHEMATIC CNTRL LISA-WIDGET 3543
050-4034-A SCH PROFILE CONTRLR LISA 2.0 0044
050-4019-A SCH.PWR.SUPP.UNIV.LISA 2213
050-4011-J SCH. PWR.SUPP.LISA 2213

LISA Microfiche

620-5103-R SUBASSY POWER SUPPLY LISA 2233
620-0220-J ASSEMBLY PCB PWR SUPPLY 8A 220V LISA 2233

699-0285-A DSK DRIVE 3 1/2 INCH SHT 1-4 1-10 0204
699-0285-A DSK DRIVE 3 1/2 INCH SHT 5-8 2-10 0204
699-0285-A DSK DRIVE 3 1/2 INCH SHT 9-12 3-10 0204
699-0285-A DSK DRIVE 3 1/2 INCH SHT 13-16 4-10 0204
699-0285-A DSK DRIVE 3 1/2 INCH SHT 17-20 5-10 0204
699-0285-A DSK DRIVE 3 1/2 INCH SHT 21-24 6-10 0204
699-0285-A DSK DRIVE 3 1/2 INCH SHT 25-28 7-10 0204
699-0285-A DSK DRIVE 3 1/2 INCH SHT 29-32 8-10 0204
699-0285-A DSK DRIVE 3 1/2 INCH SHT 33-36 9-10 0204
699-0285-A DSK DRIVE 3 1/2 INCH SHT 37-38 10-10 0204

050-0089-A SCH.MAIN LOGIC BD IMAGEWRITER SHT 1-2 3273
050-0089-A SCH.MAIN LOGIC BD IMAGEWRITER SHT 2-2 3273

699-0201-A ASSY MAIN ELECTRNC MONITOR II 3133
699-0165-A ASSY DWG, MONITOR II GRN.115V 3133
050-5020-A SCH. MAIN ELECRNCS MONITOR II DOM 3133
050-0073-C SCHEMATIC, MAIN LOGIC BRD 3183

050-5028-B SCH.R/W BD, WIDGET SHT 1-4 3253
050-5028-B SCH.R/W BD, WIDGET SHT 2-4 3253
050-5028-B SCH.R/W BD, WIDGET SHT 3-4 3253
050-5028-B SCH.R/W BD, WIDGET SHT 4-4 3253

050-4009-H SCHEMATIC CPU LISA SHT 1-5 2233
050-4009-H SCHEMATIC CPU LISA SHT 2-5 2233
050-4009-H SCHEMATIC CPU LISA SHT 3-5 2233
050-4009-H SCHEMATIC CPU LISA SHT 4-5 2233
050-4009-H SCHEMATIC CPU LISA SHT 5-5 2233

620-0117-P ASSY PCB, SYS I/O LISA 0244
620-0142-E ASSY PCH I/O BD LISA-2.0 0244
[6]20-0121-J ASSY, PCB VIDEO BRD LISA 3433
620-0121-H ASSY, PCB VIDEO BRD LISA 3363
050-4043-A SCH PCB LISA LITE ADAPTER 0044
050-4012-H SCHEMATIC VIDEO BRD LISA 3433
050-0101-A SCH.A2 MOUSE BD 0914
620-0135-B ASSY PCB PARALLEL I/F LISA 0244
620-0135-B ASSEMBLY PCB PARALLEL I/F LISA 2233

Here's a complete listing of all the files in this collection with their new ordering by DTC:

':! 21 FEBRUARY 2002:'
':! APPLE COMPUTER SCHEMATICS:'
':AppleSchematics - 400K FLOPPY:'
':AppleSchematics - APPLE 2 MAUS:'
':AppleSchematics - APPLE 2 MON:'
':AppleSchematics - IMAGEWRITER:'
':AppleSchematics - LISA:'
':AppleSchematics - MACINTOSH:'
':AppleSchematics - PROFILE HD:'
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':! 21 FEBRUARY 2002:'

':! APPLE COMPUTER SCHEMATICS:'

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':APPLE 3.5 400K DRIVE SPEC ORIG:'
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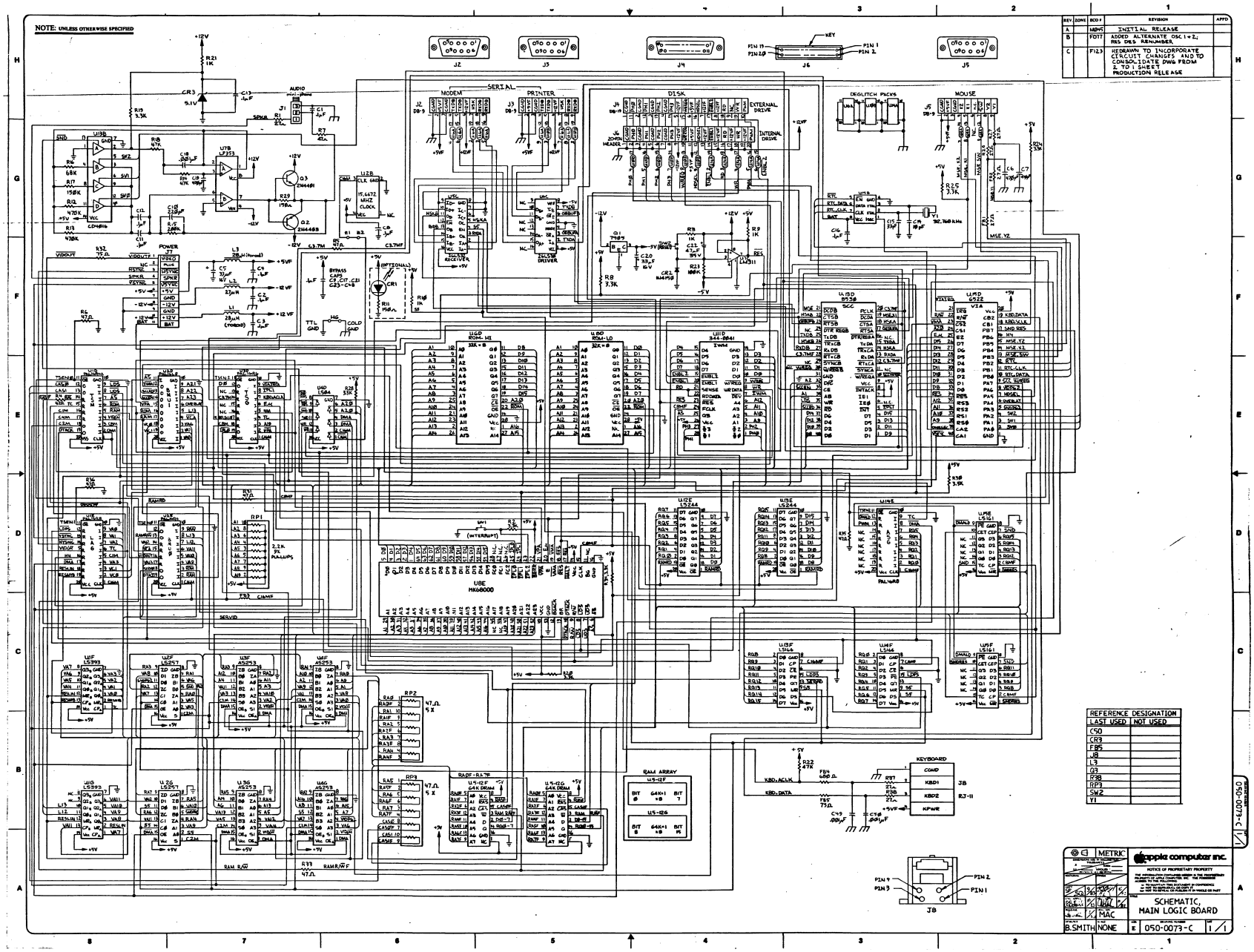
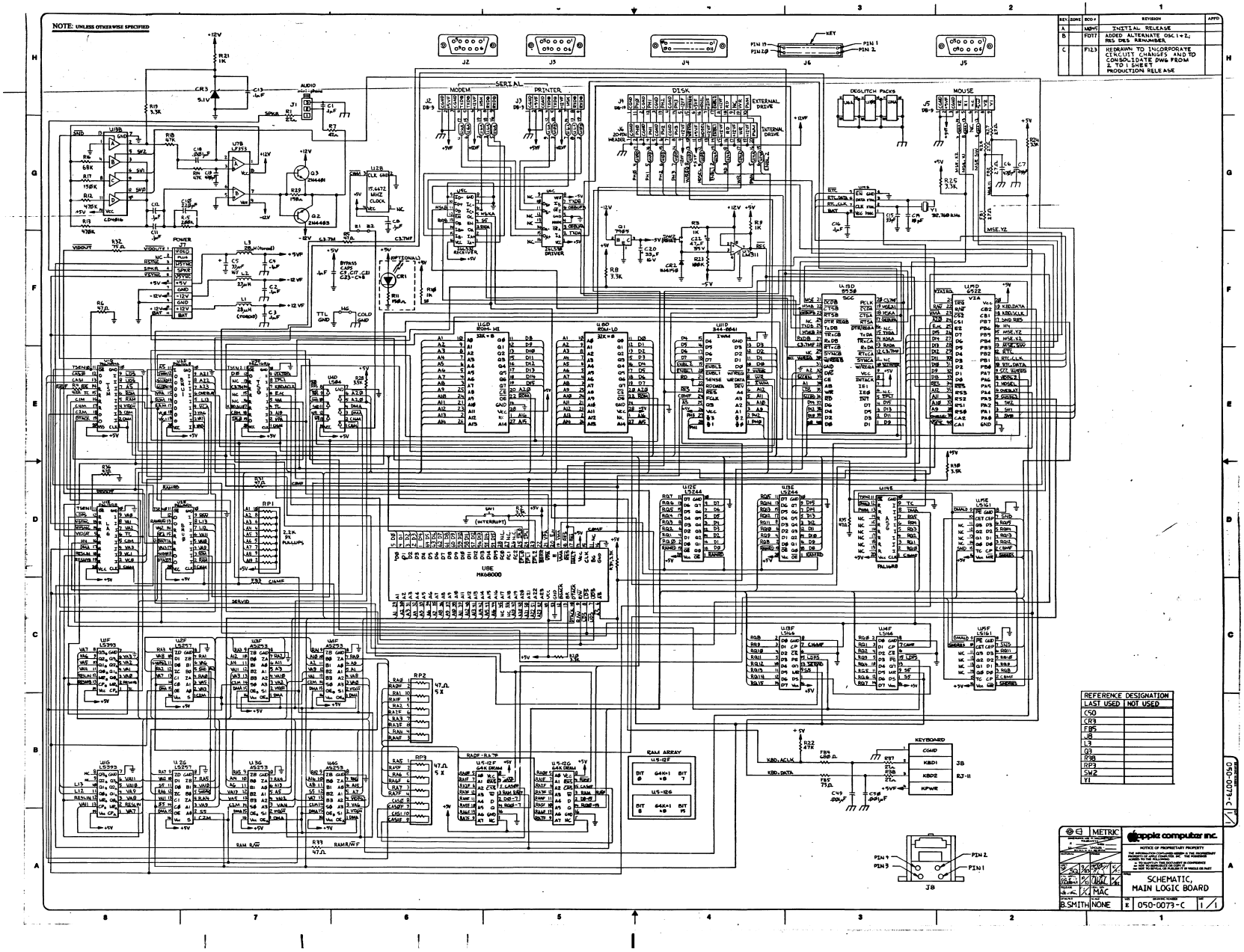
620-0~10.TIF
620-0~11.TIF
620-51~1.TIF
620-51~2.TIF
620-51~3.TIF
620-51~4.TIF
620-51~5.TIF
620-51~6.TIF
620-51~7.TIF
620-51~8.TIF
620-51~9.TIF
620-52~1.TIF
620-5~10.TIF
620-5~11.TIF
620-5~12.TIF
620-5~13.TIF
620-61~1.TIF
620-81~1.TIF
630-01~1.TIF
630-01~2.TIF
656-61~1.TIF
677-01~1.TIF
677-01~2.TIF
677-01~3.TIF
677-50~1.TIF
677-50~2.TIF
677-50~3.TIF
677-50~4.TIF
677-60~1.TIF
677-60~2.TIF
699-01~1.TIF
699-02~1.TIF
699-02~2.TIF
699-02~3.TIF
699-02~4.TIF
699-02~5.TIF
699-02~6.TIF
699-02~7.TIF
699-02~8.TIF
699-02~9.TIF
699-0~11.TIF
699-0~12.TIF
815-50~1.TIF
815-50~2.TIF

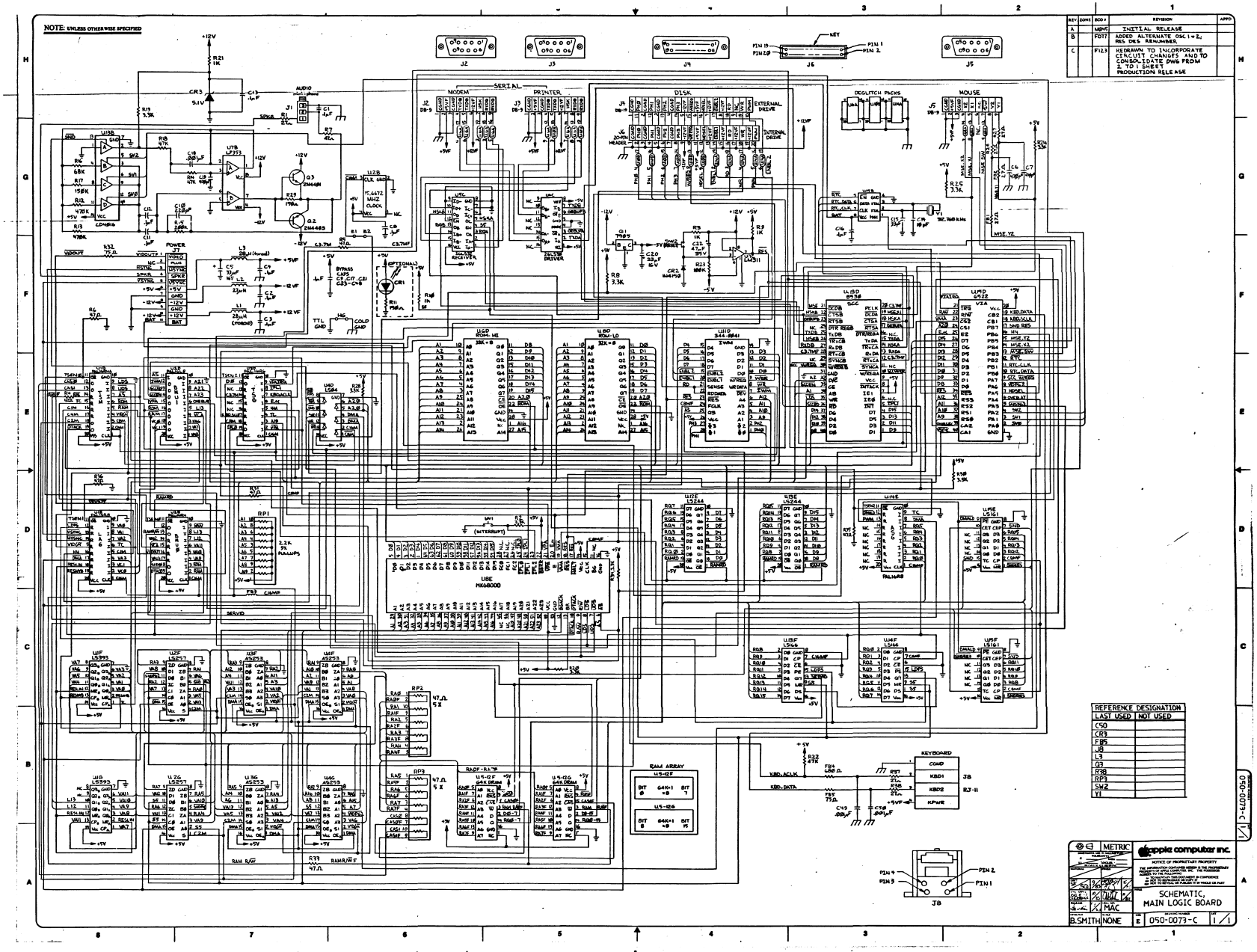
End of Document



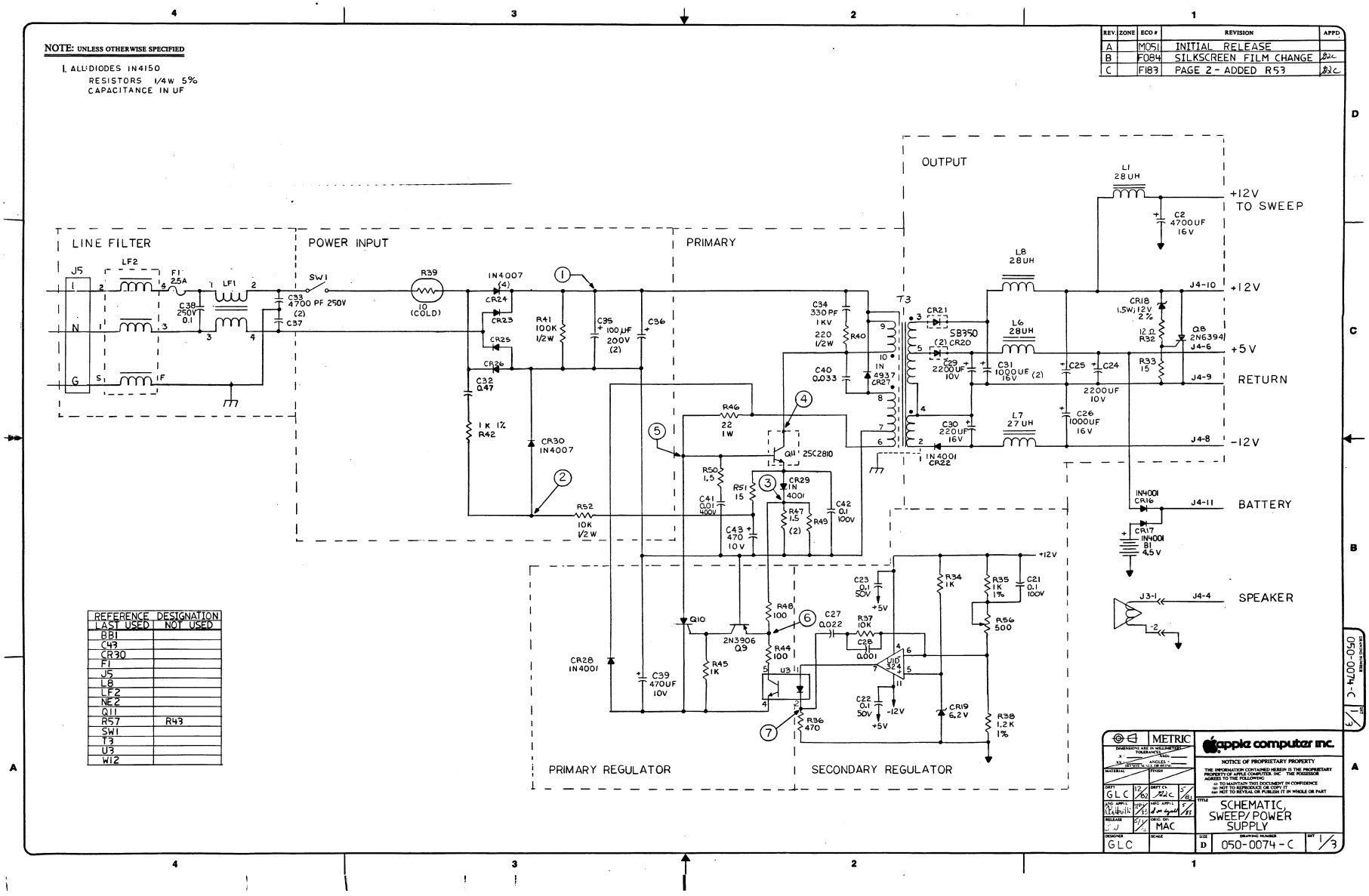
"APPLE_050-0073-C-1of1.PICT" 1866 KB 2002-03-12 dpi: 200h x 200v pix: 7833h x 5974v



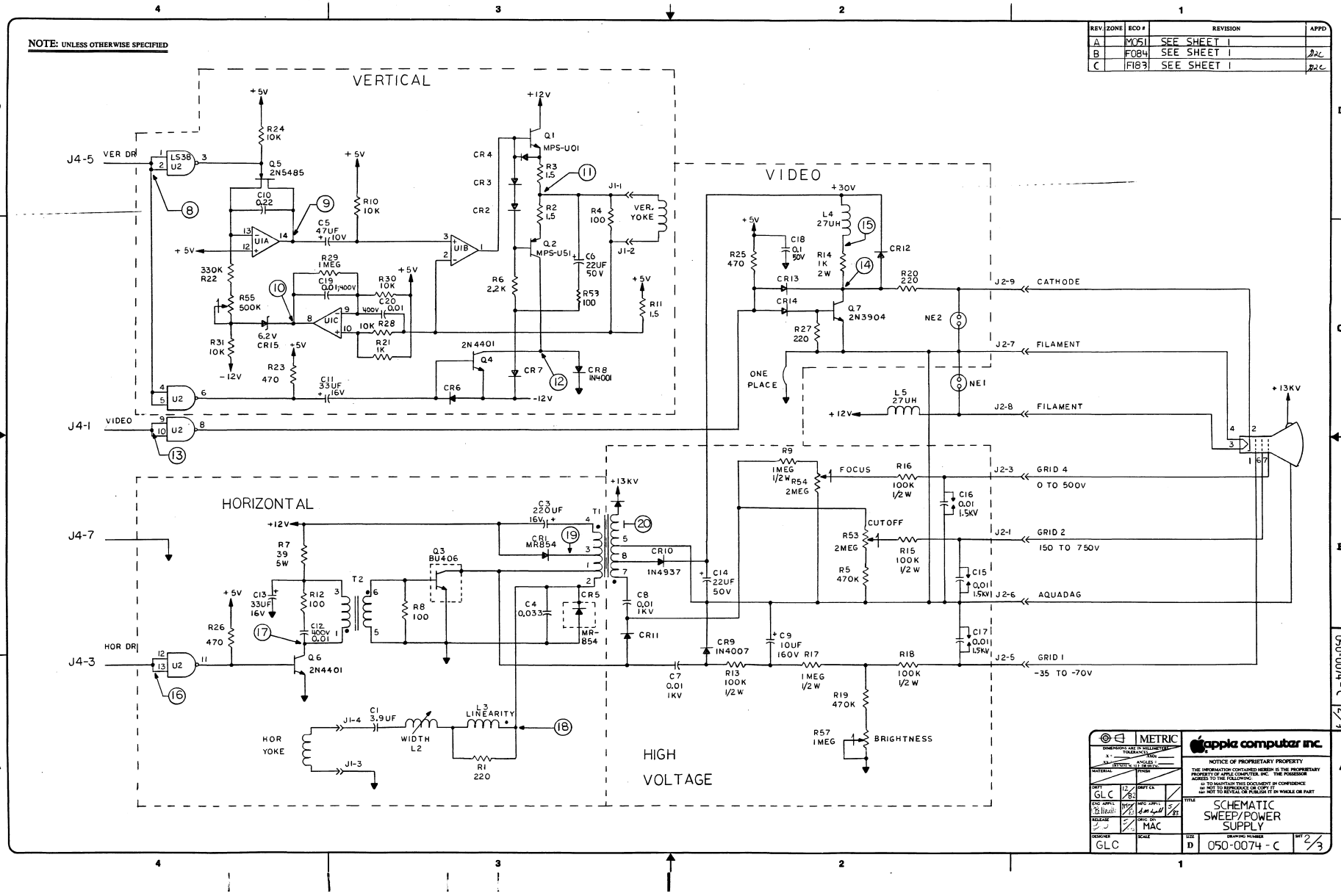
"APPLE_050-0073-C-1of1b.PICT" 1871 KB 2002-03-12 dpi: 200h x 200v pix: 8064h x 6177v



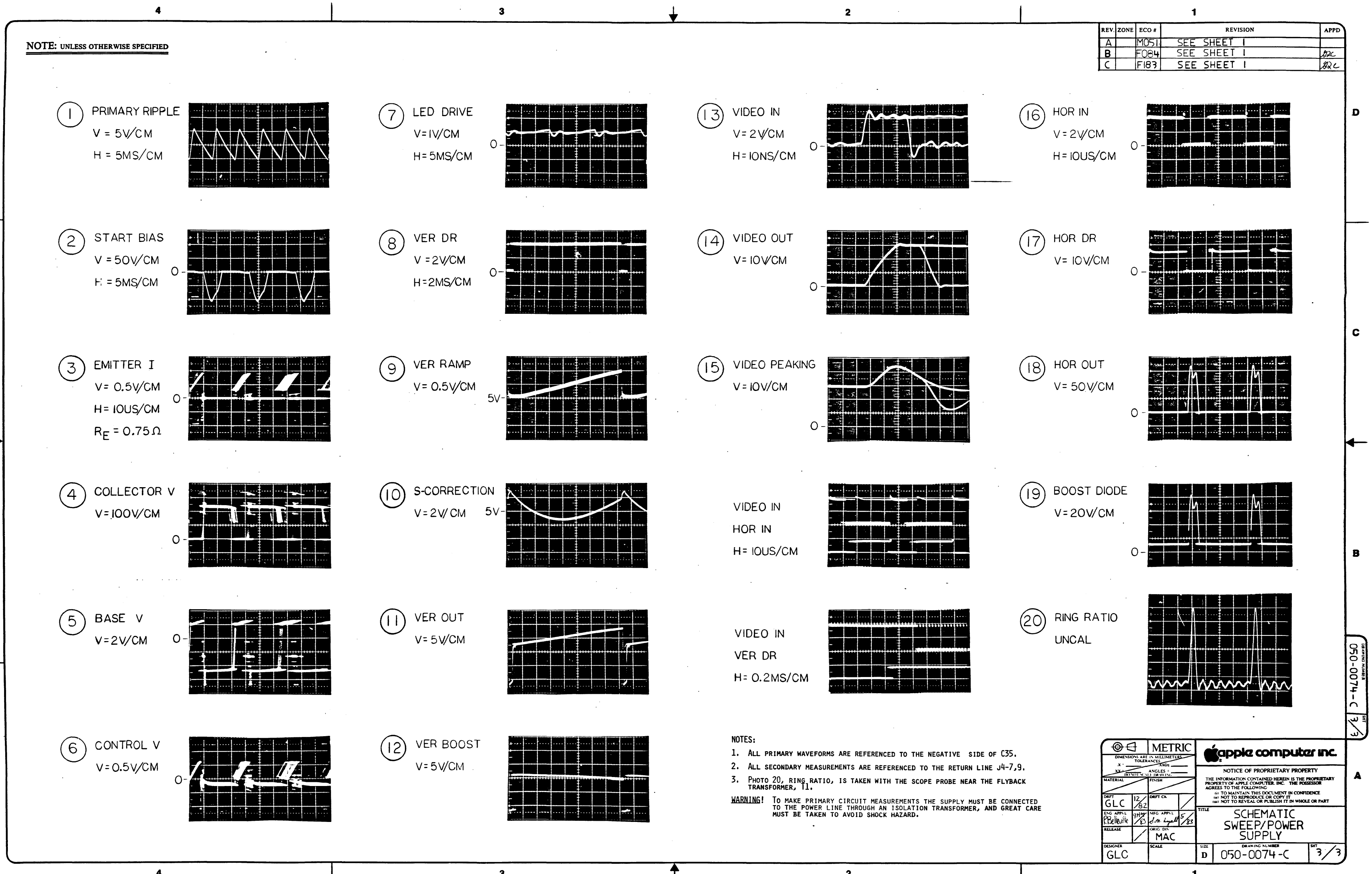
"APPLE_050-0073-C-1of1c.PICT" 1877 KB 2002-03-12 dpi: 200h x 200v pix: 7957h x 6073v



"APPLE_050-0074-C-1of3.PICT" 664 KB 2002-03-12 dpi: 200h x 200v pix: 8825h x 5615v



"APPLE_050-0074-C-2of3.PICT" 691 KB 2002-03-12 dpi: 200h x 200v pix: 8565h x 5596v



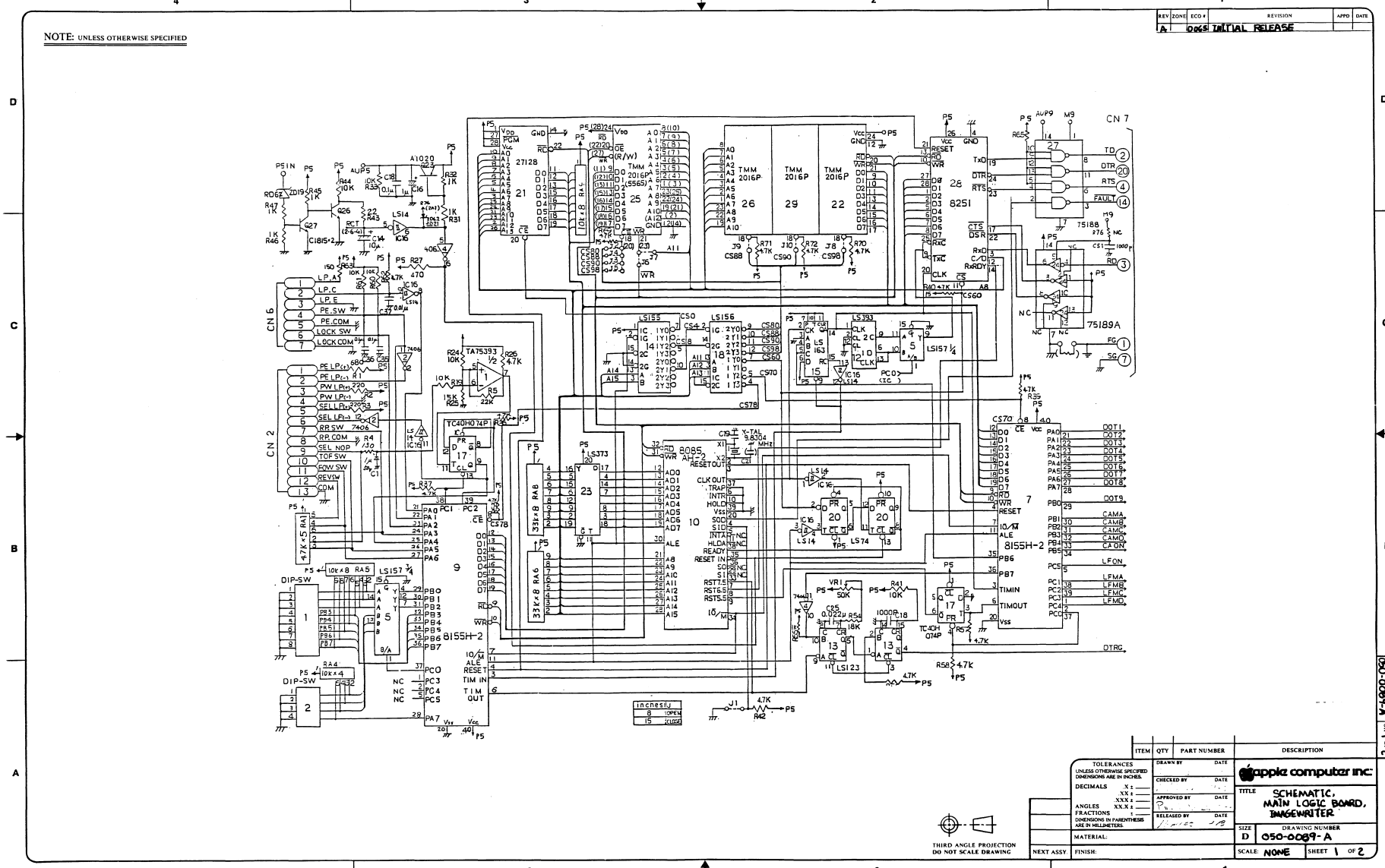
NOTES:

1. ALL PRIMARY WAVEFORMS ARE REFERENCED TO THE NEGATIVE SIDE OF C35.
2. ALL SECONDARY MEASUREMENTS ARE REFERENCED TO THE RETURN LINE J4-7,9.
3. PHOTO 20, RING RATIO, IS TAKEN WITH THE SCOPE PROBE NEAR THE FLYBACK TRANSFORMER, T1.

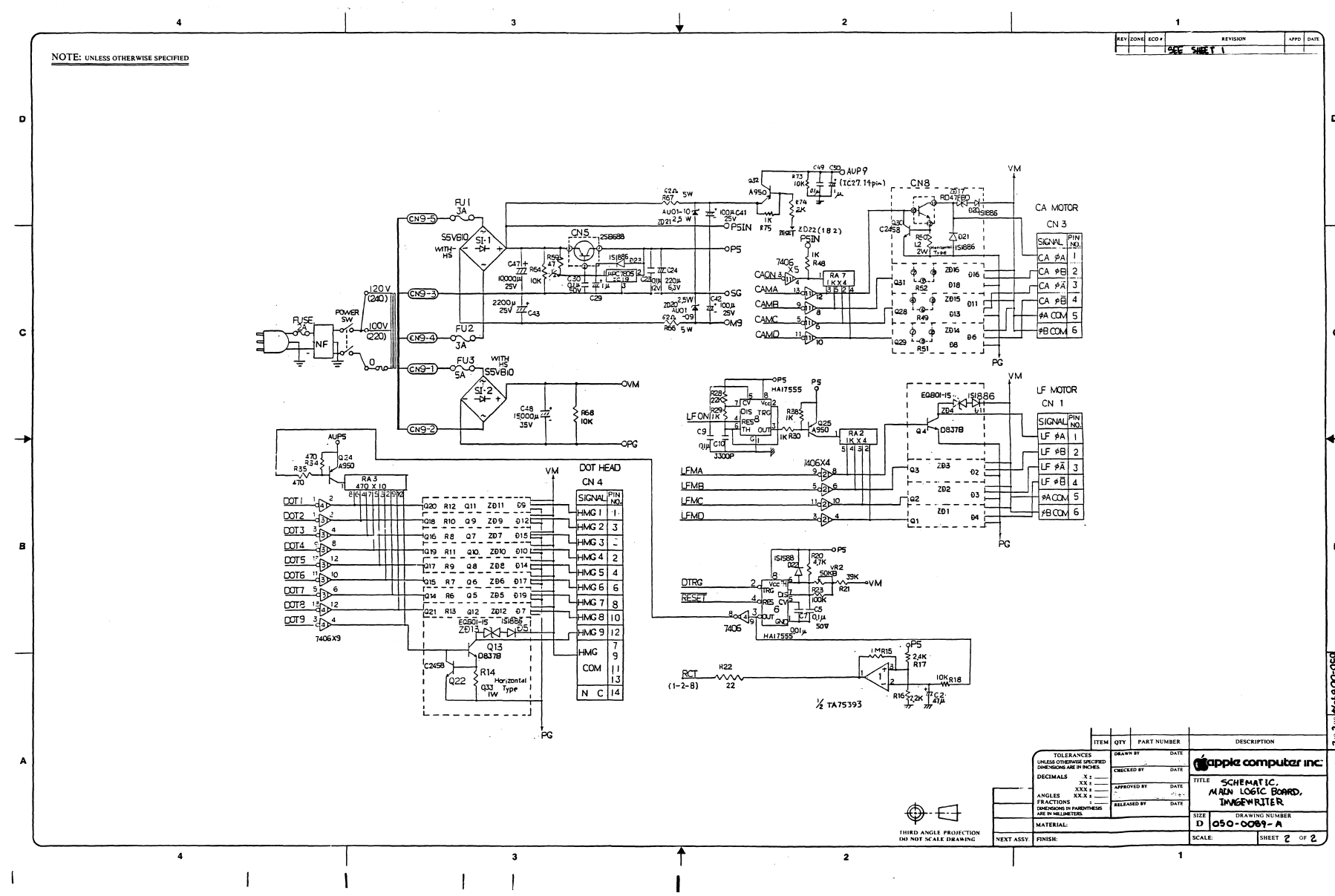
WARNING! TO MAKE PRIMARY CIRCUIT MEASUREMENTS THE SUPPLY MUST BE CONNECTED TO THE POWER LINE THROUGH AN ISOLATION TRANSFORMER, AND GREAT CARE MUST BE TAKEN TO AVOID SHOCK HAZARD.

METRIC		apple computer inc.	
DIMENSIONS ARE IN MILLIMETERS TOLERANCES .X = .XX = .XXX = ANGLES = DO NOT SCALE DRAWING		NOTICE OF PROPRIETARY PROPERTY	
MATERIAL	FINISH	THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: (i) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE (ii) NOT TO REPRODUCE OR COPY IT (iii) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART	
DRFT GLC 12/82	DRFT CK	TITLE SCHEMATIC SWEEP/POWER SUPPLY	
ENG APPVL R Belleville 9 May 83	MFG APPVL S.M. Lyall 5/83		
RELEASE	ORIG. DIV MAC		
DESIGNER GLC	SCALE	SIZE D DRAWING NUMBER 050-0074-C	SHT 3/3

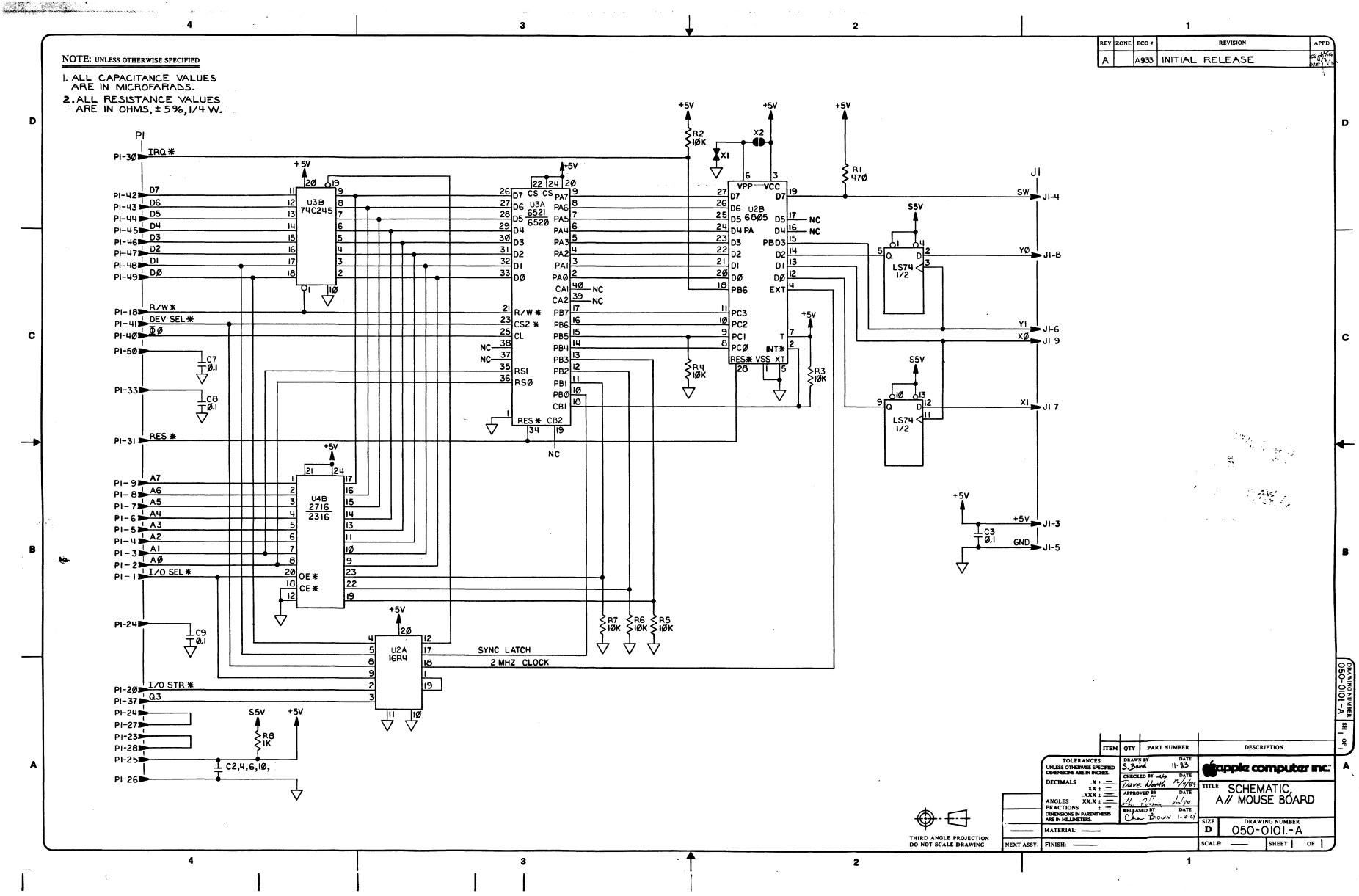
“APPLE_050-0074-C-3of3.PICT” 1015 KB 2002-03-12 dpi: 200h x 200v pix: 8587h x 5574v



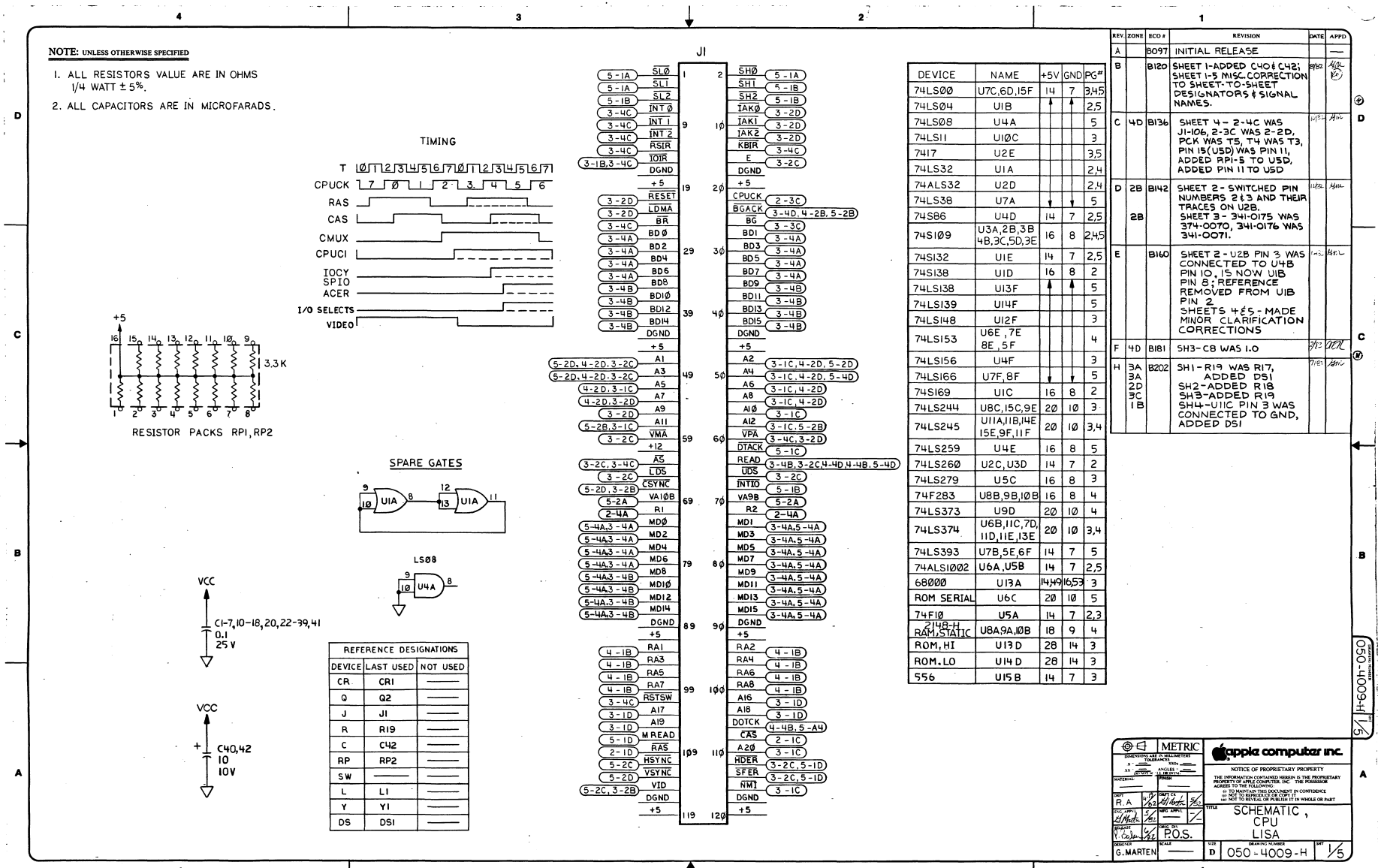
"APPLE_050-0089-A-1of2.PICT" 1069 KB 2002-03-12 dpi: 200h x 200v pix: 8655h x 5558v



"APPLE_050-0089-A-2of2.PICT" 712 KB 2002-03-12 dpi: 200h x 200v pix: 8842h x 5770v



"APPLE_050-0101-A-1of1.PICT" 711 KB 2002-03-12 dpi: 200h x 200v pix: 8712h x 5617v


NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS VALUE ARE IN OHMS 1/4 WATT ± 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
TIMING
T Ø 1 2 3 4 5 6 7 Ø 1 2 3 4 5 6 7
CPUCK 7 Ø 1 2 3 4 5 6
RAS
CAS
CMUX
CPUCI
IOCY
SPIO
ACER
I/O SELECTS
VIDEO
+5
3.3K
RESISTOR PACKS RP1, RP2
SPARE GATES
U1A
LS08
U4A
VCC
C1-7,10-18,20,22-39,41 0.1 25V
C40,42 10 10V
J1
SLØ SL1 SL2 INTØ INT1 INT2 RSIR IOTR DGND +5 RESET LDMA BR BDØ BD2 BD4 BD6 BDØ BDI2 BDI4 DGND +5 A1 A3 A5 A7 A9 A11 VMA +12 AS LDS CSYNC VAIØB R1 MDØ MD2 MD4 MD6 MD8 MDIØ MDI2 MDI4 DGND +5 RA1 RA3 RA5 RA7 RSTSW A17 A19 M READ RAS HSYNC VSYNC VID DGND +5
SHØ SH1 SH2 IAKØ IAK1 IAK2 KBIR E DGND +5 CPUCK BGACK BG BD1 BD3 BD5 BD7 BD9 BDI1 BDI3 BDI5 DGND +5 A2 A4 A6 A8 AIØ AI2 VPA DTACK READ UDS INTIO VA9B R2 MDI MD3 MD5 MD7 MD9 MDI1 MDI3 MDI5 DGND +5 RA2 RA4 RA6 RA8 A16 A18 DOTCK CAS A2Ø HDER SFER NMI DGND +5
REFERENCE DESIGNATIONS
DEVICE LAST USED NOT USED
CR CR1
Q Q2
J J1
R R19
C C42
RP RP2
SW
L L1
Y Y1
DS DS1
DEVICE NAME +5V GND PG#
74LSØØ U7C,6D,15F 14 7 3,4,5
74LSØ4 U1B 2,5
74LSØ8 U4A 5
74LS11 U1ØC 3
7417 U2E 3,5
74LS32 U1A 2,4
74ALS32 U2D 2,4
74LS38 U7A 5
74S86 U4D 14 7 2,5
74S1Ø9 U3A,2B,3B 4B,3C,5D,3E 16 8 2,4,5
74S132 U1E 14 7 2,5
74S138 U1D 16 8 2
74LS138 U13F 5
74LS139 U14F 5
74LS148 U12F 3
74LS153 U6E,7E 8E,5F 4
74LS156 U4F 3
74LS166 U7F,8F 5
74S169 U1C 16 8 2
74LS244 U8C,15C,9E 2Ø 1Ø 3
74LS245 U11A,11B,14E 15E,9F,11F 2Ø 1Ø 3,4
74LS259 U4E 16 8 5
74LS26Ø U2C,U3D 14 7 2
74LS279 U5C 16 8 3
74F283 U8B,9B,1ØB 16 8 4
74LS373 U9D 2Ø 1Ø 4
74LS374 U6B,11C,7D 11D,11E,13E 2Ø 1Ø 3,4
74LS393 U7B,5E,6F 14 7 5
74ALS1Ø02 U6A,U5B 14 7 2,5
68ØØØ U13A 14,49 16,53 3
ROM SERIAL U6C 2Ø 1Ø 5
74F1Ø 2148-H RAM,STATIC U5A U8A,9A,1ØB 14 18 7 9 2,3 4
ROM,HI U13D 28 14 3
ROM.LO U14D 28 14 3
556 U15B 14 7 3
REV ZONE ECO # REVISION DATE APPD
A B097 INITIAL RELEASE
B B120 SHEET 1-ADDED C40 & C42; SHEET 1-5 MISC. CORRECTION TO SHEET-TO-SHEET DESIGNATORS & SIGNAL NAMES.
C 4D B136 SHEET 4 - 2-4C WAS J1-106, 2-3C WAS 2-2D, PCK WAS T5, T4 WAS T3, PIN 15(U5D) WAS PIN 11, ADDED RP1-5 TO U5D, ADDED PIN 11 TO U5D
D 2B B142 SHEET 2 - SWITCHED PIN NUMBERS 2 & 3 AND THEIR TRACES ON U2B.
2B SHEET 3 - 341-0175 WAS 374-0070, 341-0176 WAS 341-0071.
E B160 SHEET 2 - U2B PIN 3 WAS CONNECTED TO U4B PIN 10, IS NOW U1B PIN 8; REFERENCE REMOVED FROM U1B PIN 2.
SHEETS 4 & 5 - MADE MINOR CLARIFICATION CORRECTIONS
F 4D B181 SH3-C8 WAS 1.0
H 3A B202 SH1-R19 WAS R17, ADDED D51
3A SH2-ADDED R18
2D SH3-ADDED R19
3C SH4-U11C PIN 3 WAS CONNECTED TO GND, ADDED D51
1B
METRIC
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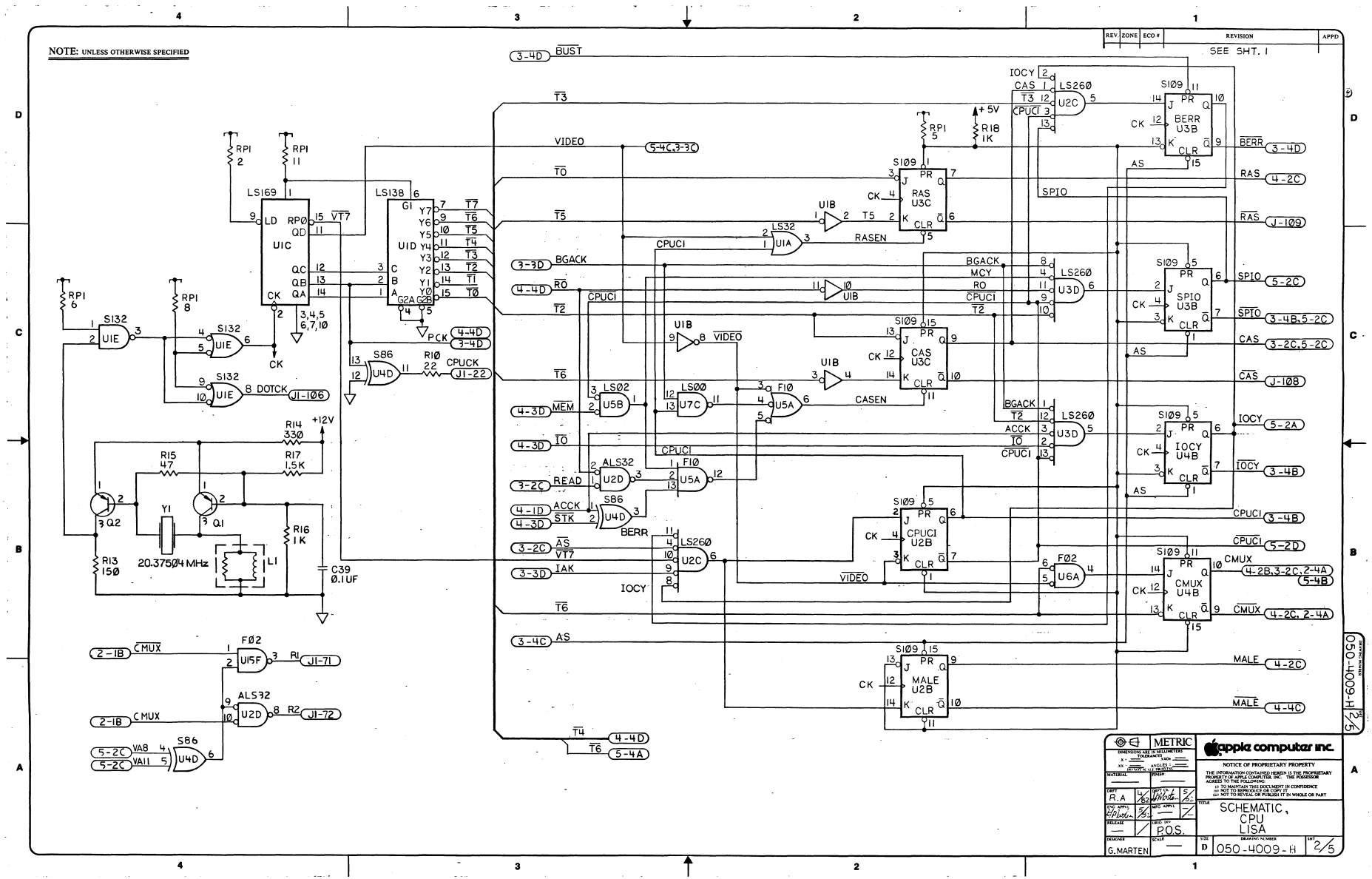
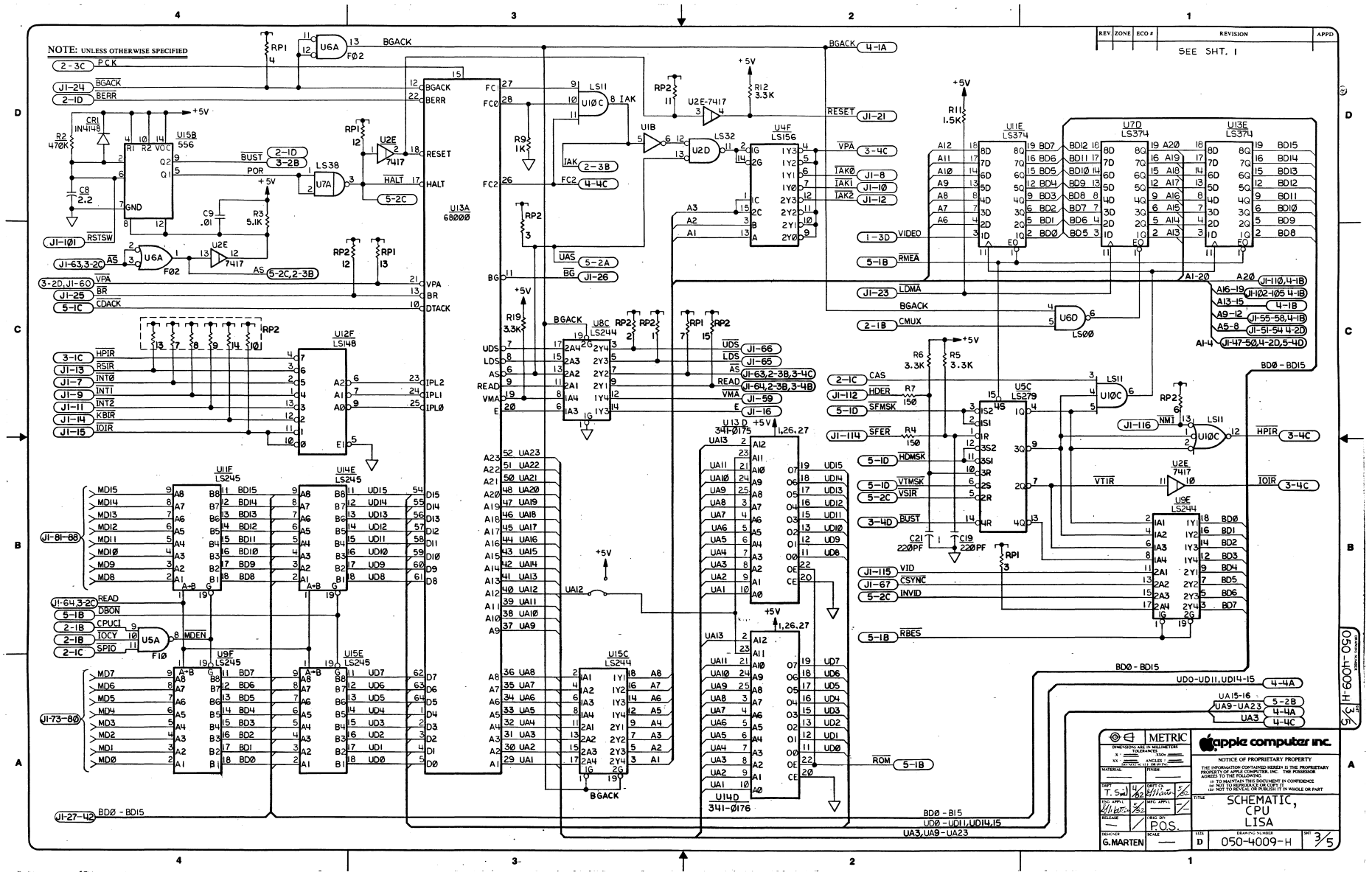
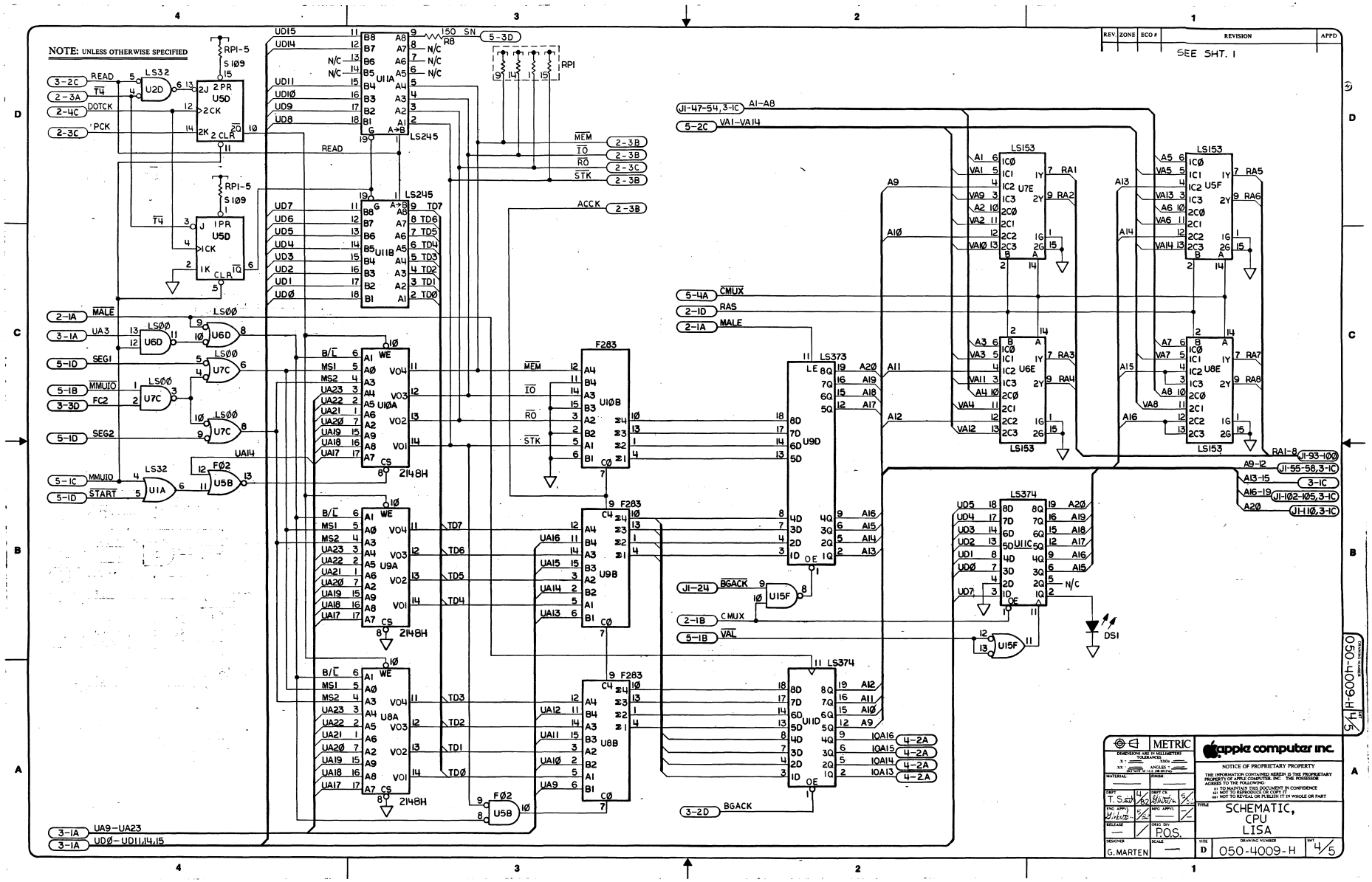
R.A
P.O.S.
G. MARTEN
SCHEMATIC, CPU LISA
D
050-4009-H
1/5
050-4009-H



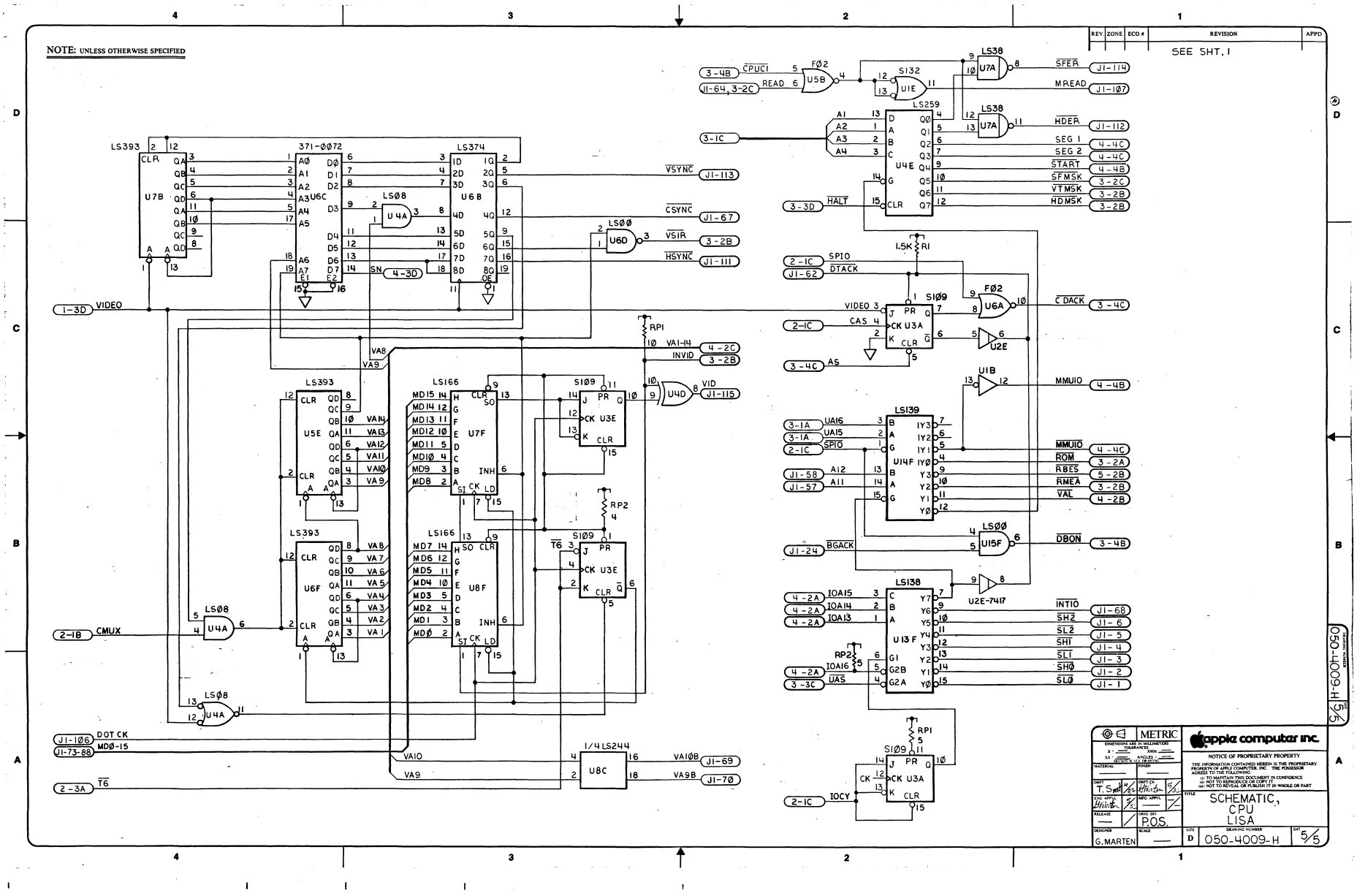
"APPLE_050-4009-H-2of5.PICT" 867 KB 2002-03-12 dpi: 200h x 200v pix: 8657h x 5634v



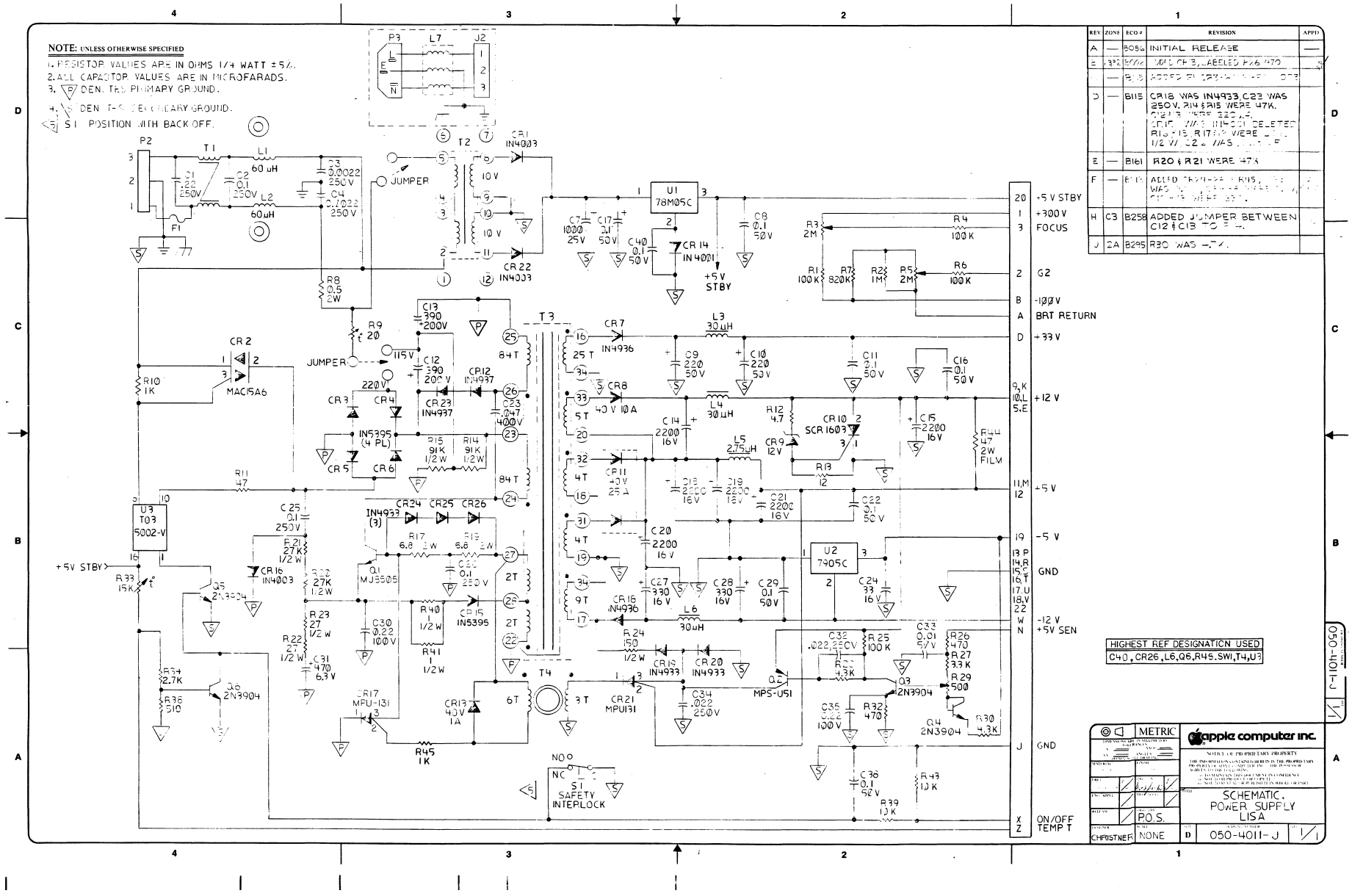
"APPLE_050-4009-H-3of5.PICT" 1288 KB 2002-03-12 dpi: 200h x 200v pix: 8649h x 5637v



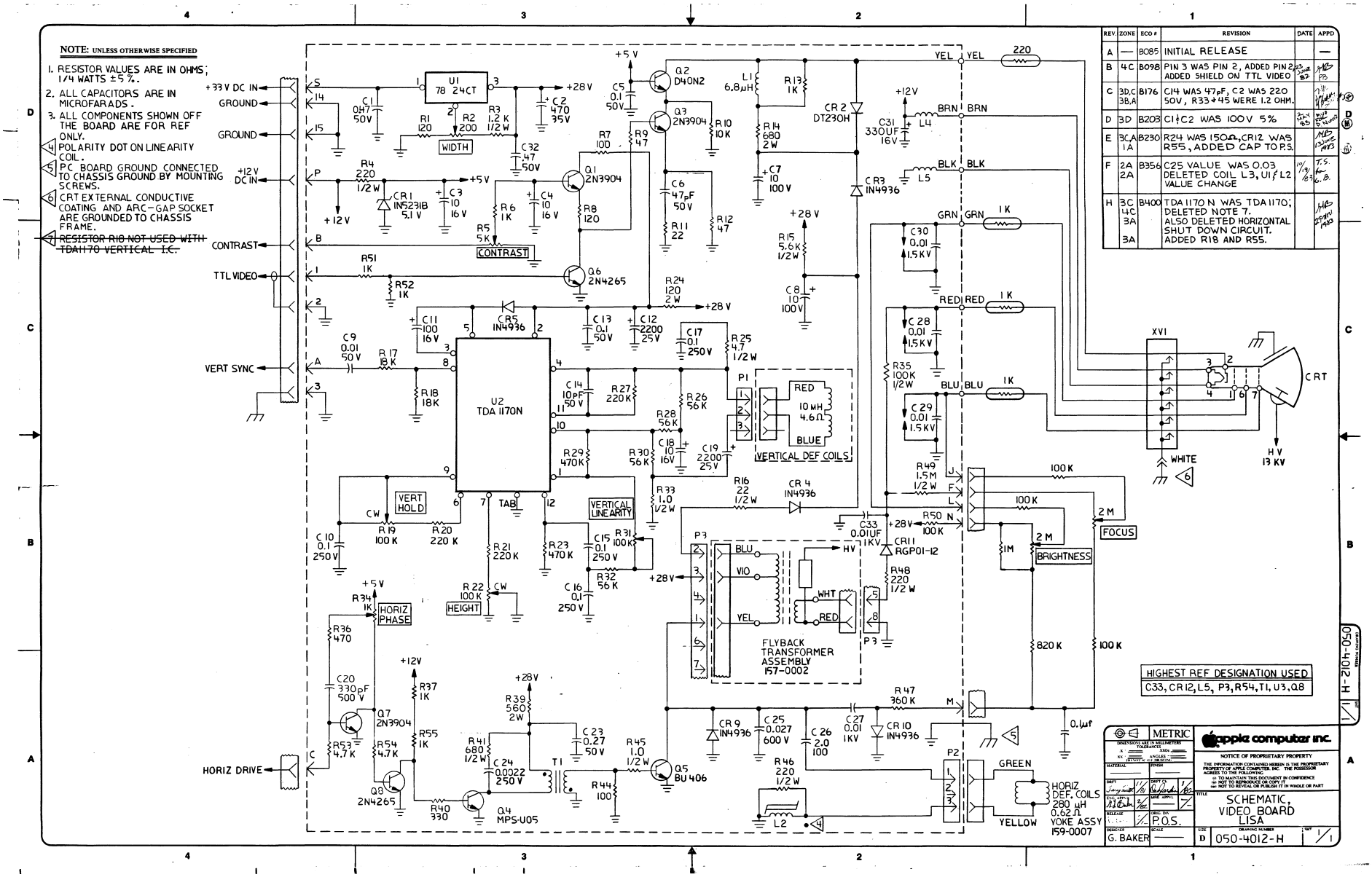
"APPLE_050-4009-H-4of5.PICT" 1140 KB 2002-03-12 dpi: 200h x 200v pix: 8610h x 5721v



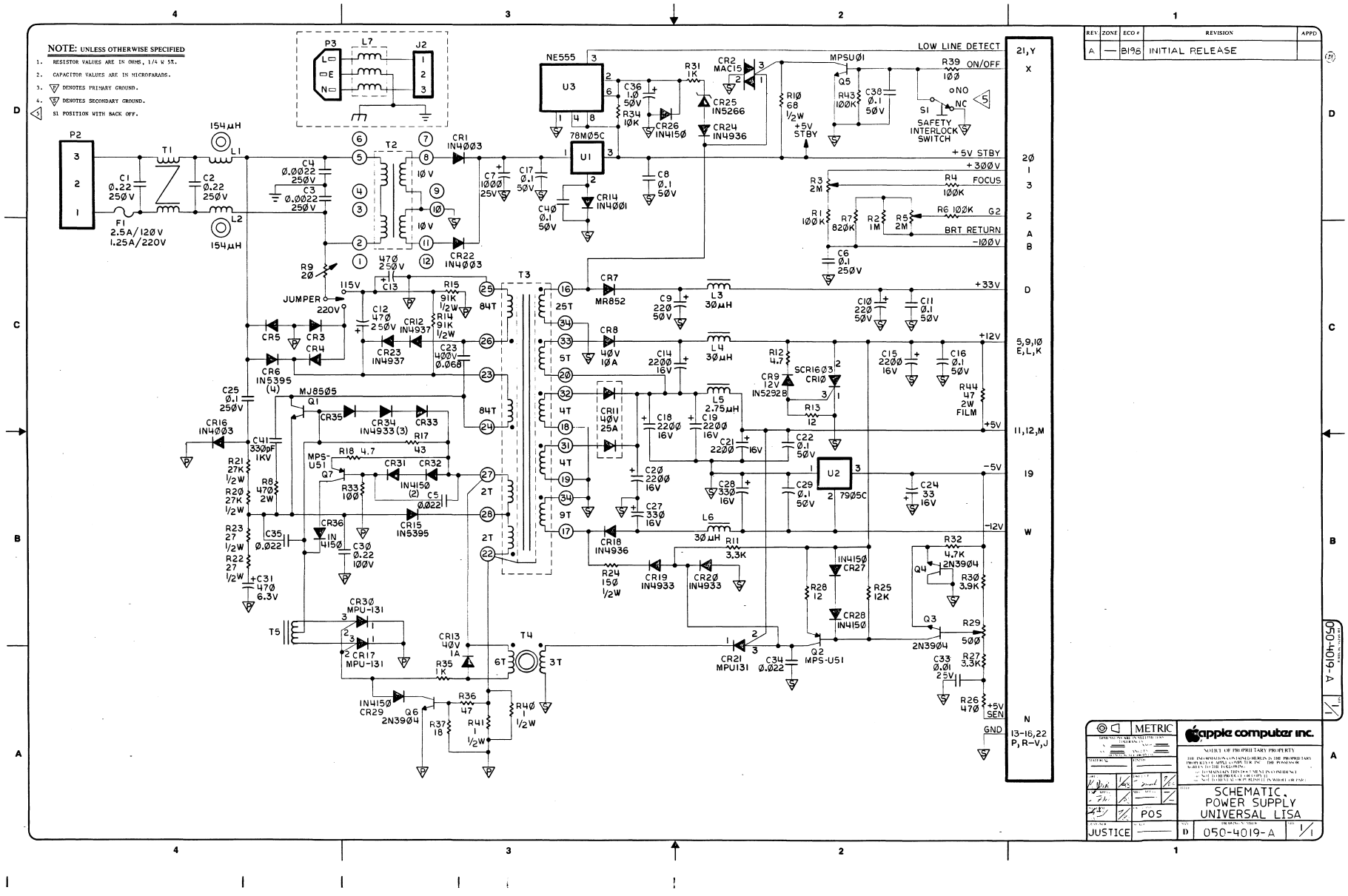
"APPLE_050-4009-H-5of5.PICT" 869 KB 2002-03-12 dpi: 200h x 200v pix: 8627h x 5686v



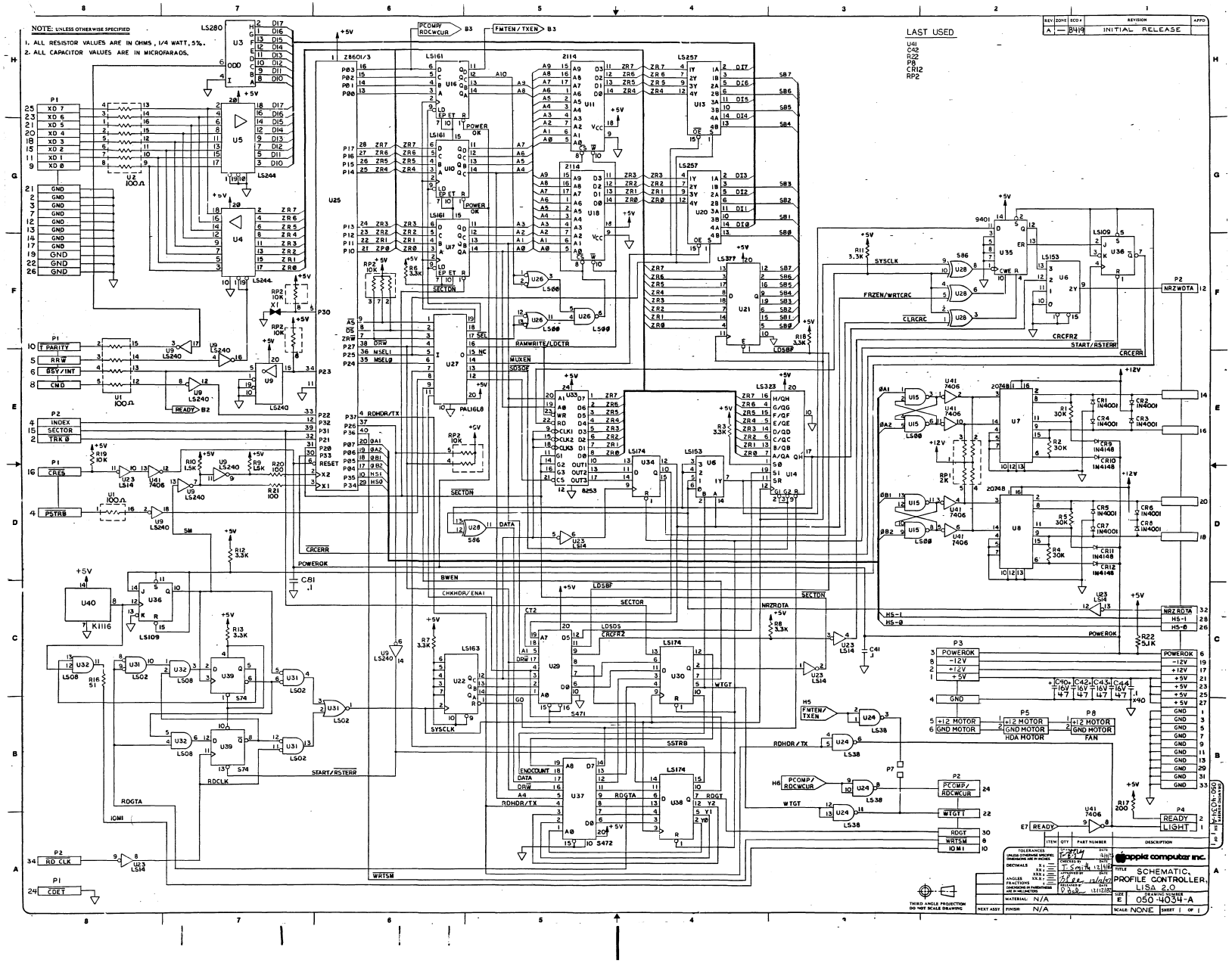
"APPLE_050-4011-J-1of1.PICT" 921 KB 2002-03-12 dpi: 200h x 200v pix: 8663h x 5712v



REV.	ZONE	ECO #	REVISION	DATE	APPD
A	—	B085	INITIAL RELEASE		—
B	4C	B098	PIN 3 WAS PIN 2, ADDED PIN 2 ADDED SHIELD ON TTL VIDEO		
C	3D,C 3B,A	B176	C14 WAS 47pF, C2 WAS 220 50V, R33+45 WERE 1.2 OHM.		
D	3D	B203	C1+C2 WAS 100V 5%		
E	3C,A 1A	B230	R24 WAS 150Ω, CR12 WAS R55, ADDED CAP TO P.S.		
F	2A 2A	B356	C25 VALUE WAS 0.03 DELETED COIL L3, U1 & L2 VALUE CHANGE		
H	3C 4C 3A 3A	B400	TDA 1170 N WAS TDA 1170; DELETED NOTE 7. ALSO DELETED HORIZONTAL SHUT DOWN CIRCUIT. ADDED R18 AND R55.		



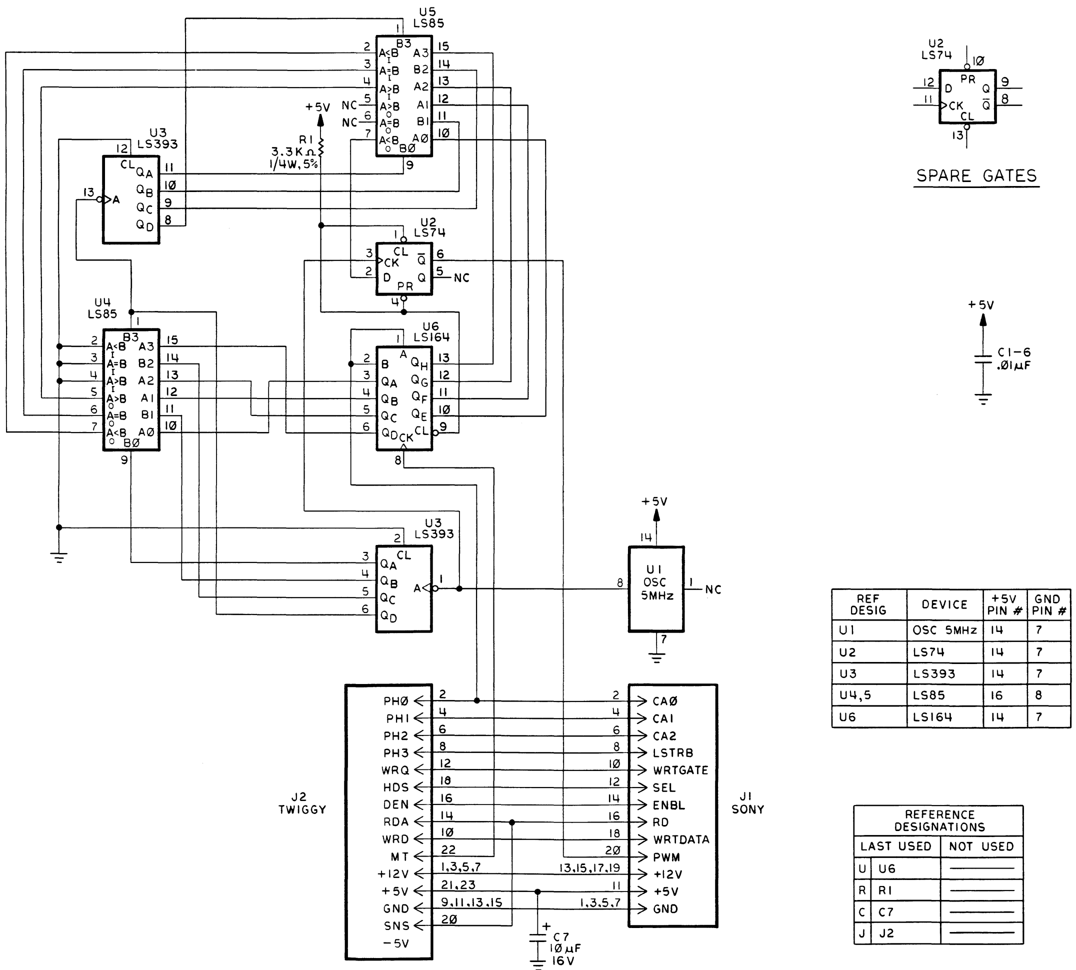
"APPLE_050-4019-A-1of1.PICT" 934 KB 2002-03-12 dpi: 200h x 200v pix: 8784h x 5740v



"APPLE_050-4034-A-1of1.PICT" 1440 KB 2002-03-12 dpi: 200h x 200v pix: 8071h x 6090v

REV	ZONE	ECO #	REVISION	APP'D	DATE
A	—	8449	INITIAL RELEASE		

NOTE: UNLESS OTHERWISE SPECIFIED



REF DESIG	DEVICE	+5V PIN #	GND PIN #
U1	OSC 5MHz	14	7
U2	LS74	14	7
U3	LS393	14	7
U4,5	LS85	16	8
U6	LS164	14	7

REFERENCE DESIGNATIONS

	LAST USED	NOT USED
U	U6	———
R	R1	———
C	C7	———
J	J2	———

METRIC

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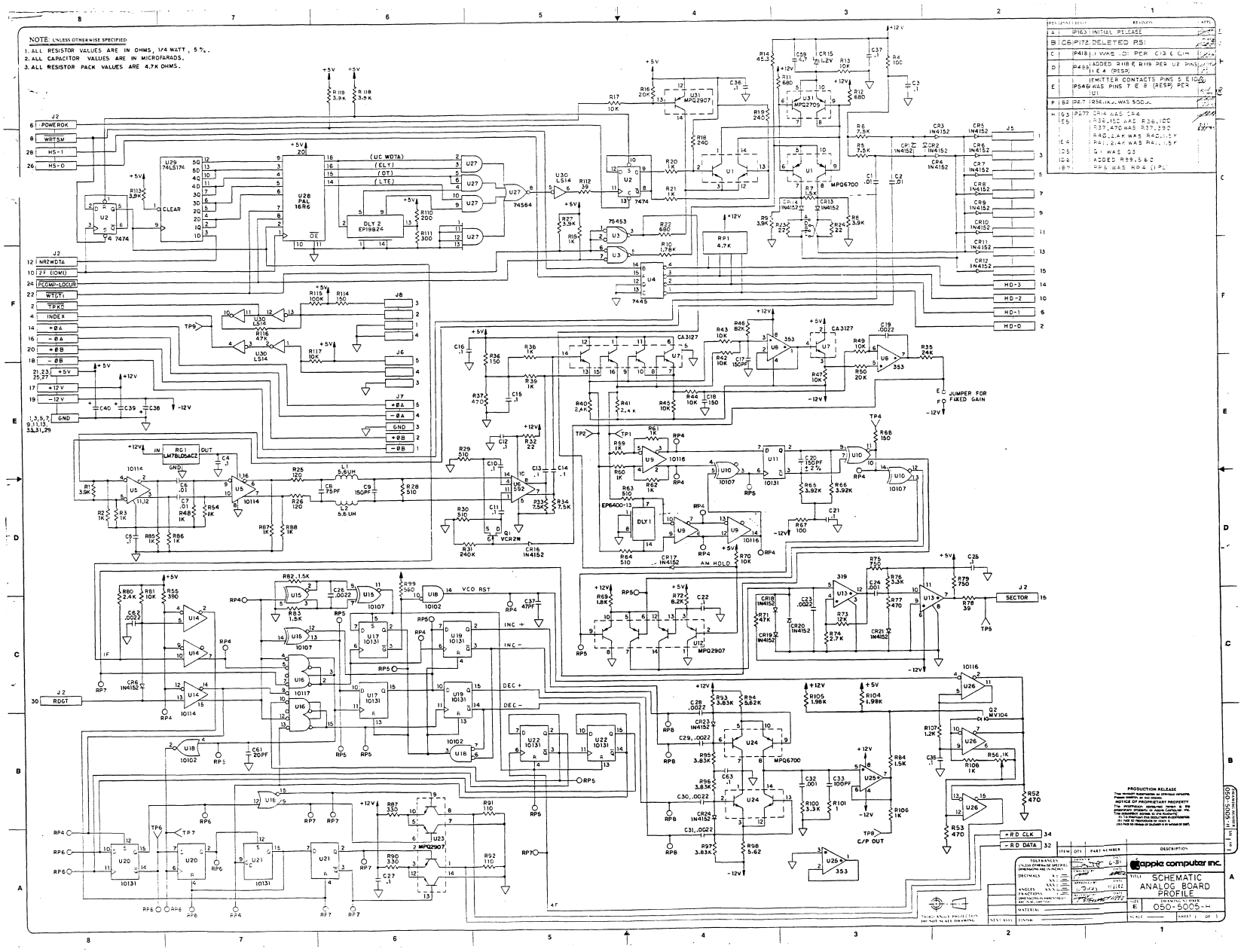
DRFT: K. Jenks · DESIGNER: B. LEE · LISA

TITLE: SCHEMATIC, PCB, LISA LITE ADAPTOR

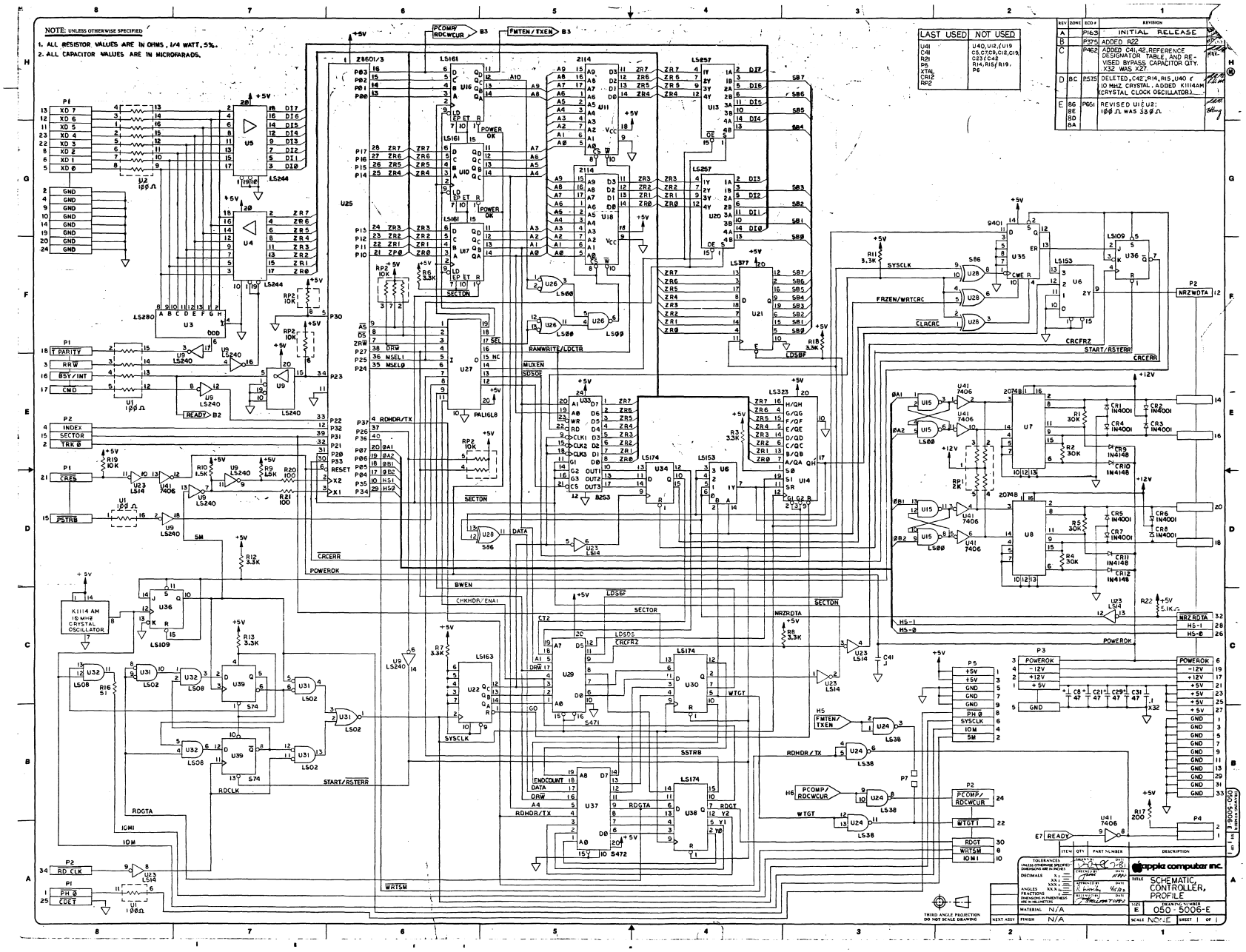
SIZE: D · DRAWING NUMBER: 050-4043-A · SHT 1/1

050-4043-A 1/1

“APPLE_050-4043-A-1of1.PICT” 563 KB 2002-03-12 dpi: 200h x 200v pix: 8448h x 5566v



"APPLE_050-5005-H-1of1.PICT" 1002 KB 2002-03-12 dpi: 200h x 200v pix: 7273h x 5610v

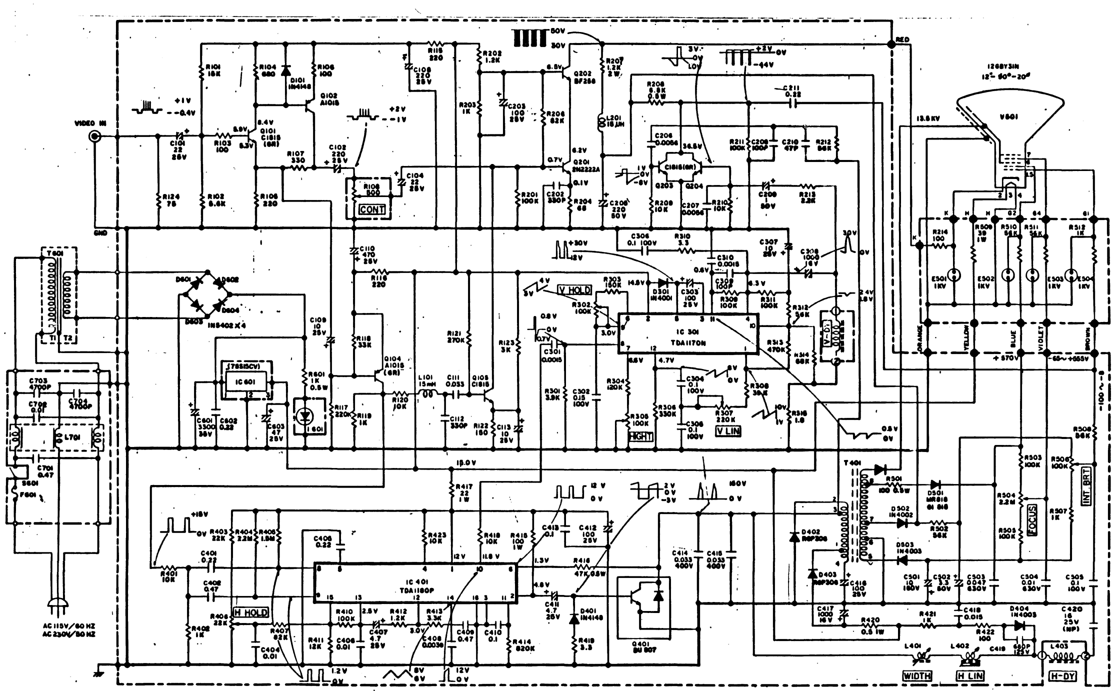


"APPLE_050-5006-E-1of1.PICT" 1576 KB 2002-03-12 dpi: 200h x 200v pix: 7932h x 5995v

REV.	ZONE	ECO #	REVISION	APPD
A		D071	INITIAL RELEASE	

NOTE: UNLESS OTHERWISE SPECIFIED

1. ○ DENOTES HOUSING CONNECTOR
2. ● DIRECT
3. ALL WAVEFORMS MEASURED WITH STRONG SIGNAL INPUT. CONTRAST SET TO GIVE NORMAL PICTURE.



METRIC

DIMENSIONS ARE IN MILLIMETERS
TOLERANCES
.X ± .XXX±
.XX ± ANGLES ±
DO NOT SCALE DRAWING

MATERIAL: FINISH:

DRFT	M.WONG	7/83	DRFT CK	B. Muys	10/83
ENG APPVL		10/83	MFG APPVL		
RELEASE	V.Waller	11/83	ORIG. DIV	APG	
DESIGNER			SCALE	NONE	

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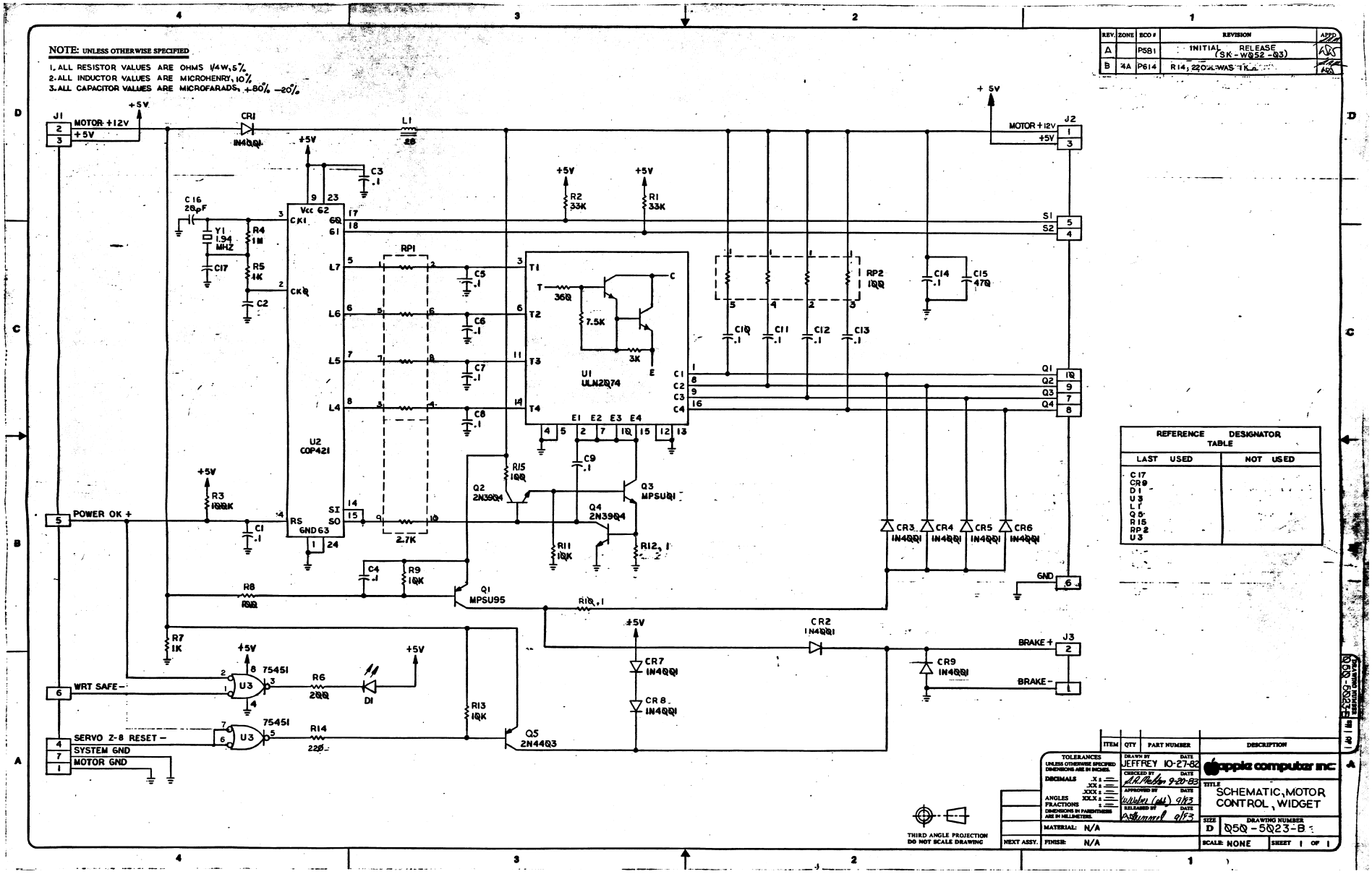
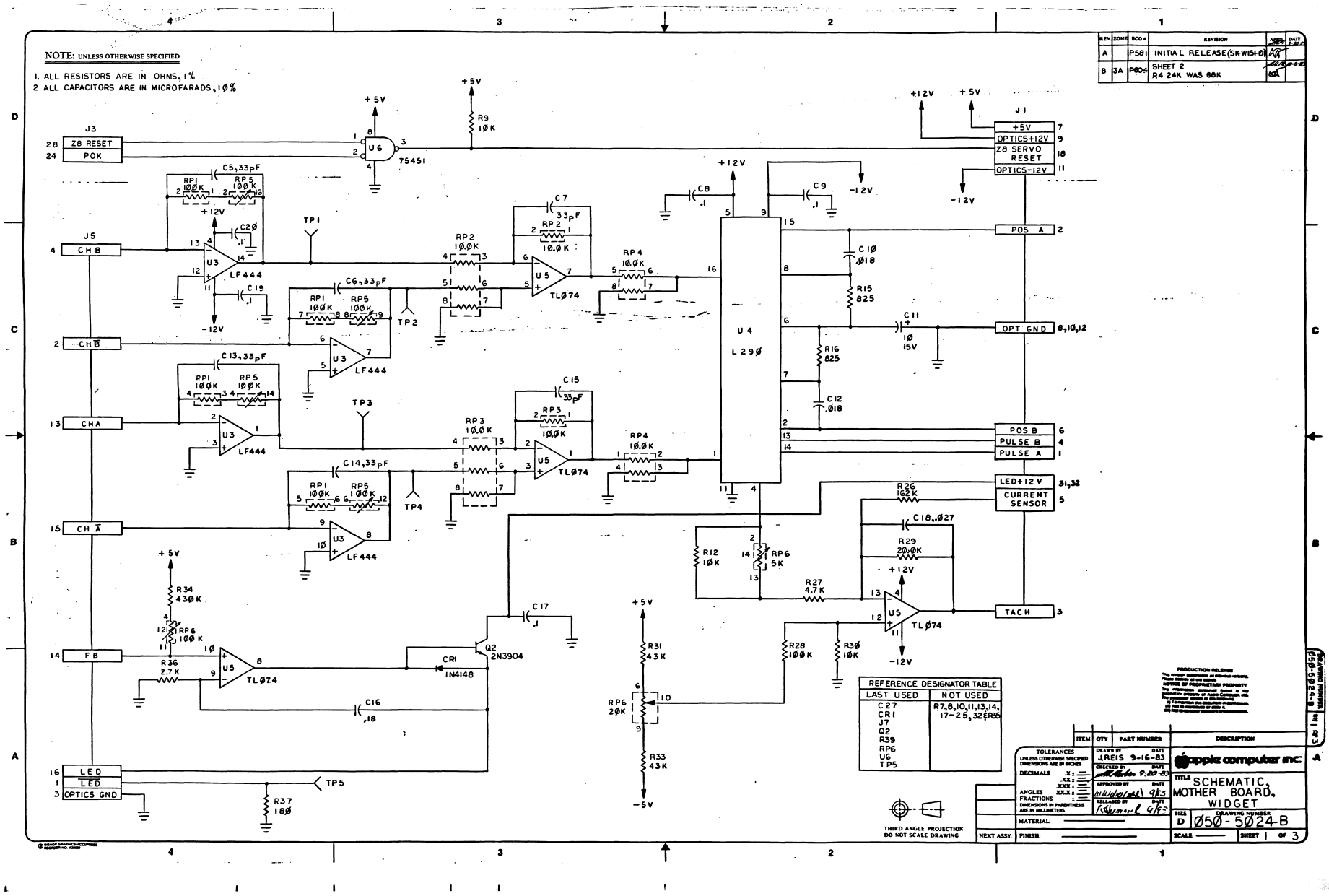
TITLE: SCHEMATIC, MAIN ELECTRONICS, MONITOR II, DOMESTIC

SIZE: C DRAWING NUMBER: 050-5020-A SHT: 1/1

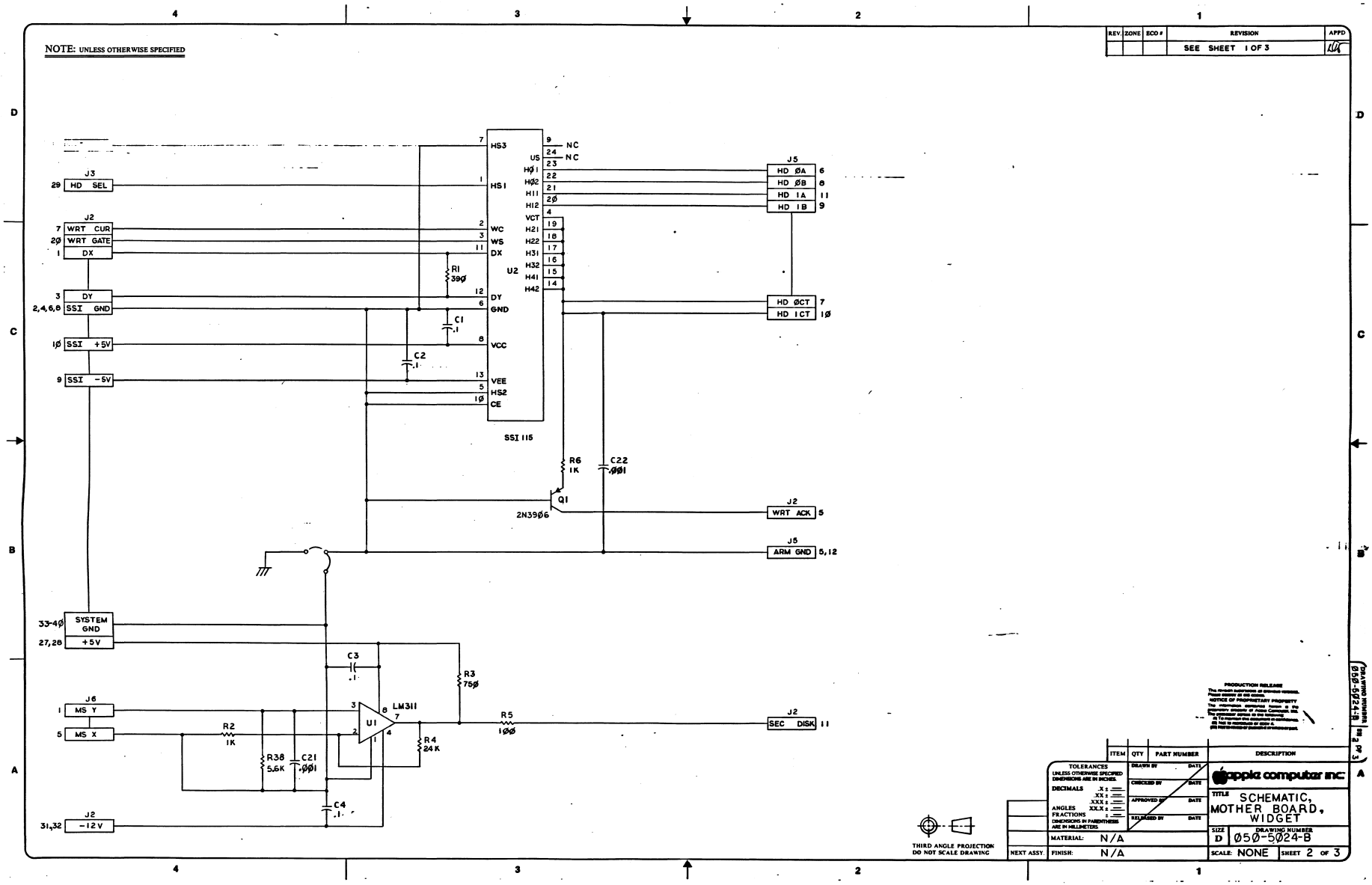
“APPLE_050-5020-A-1of1.PICT” 1063 KB 2002-03-12 dpi: 200h x 200v pix: 8265h x 6446v



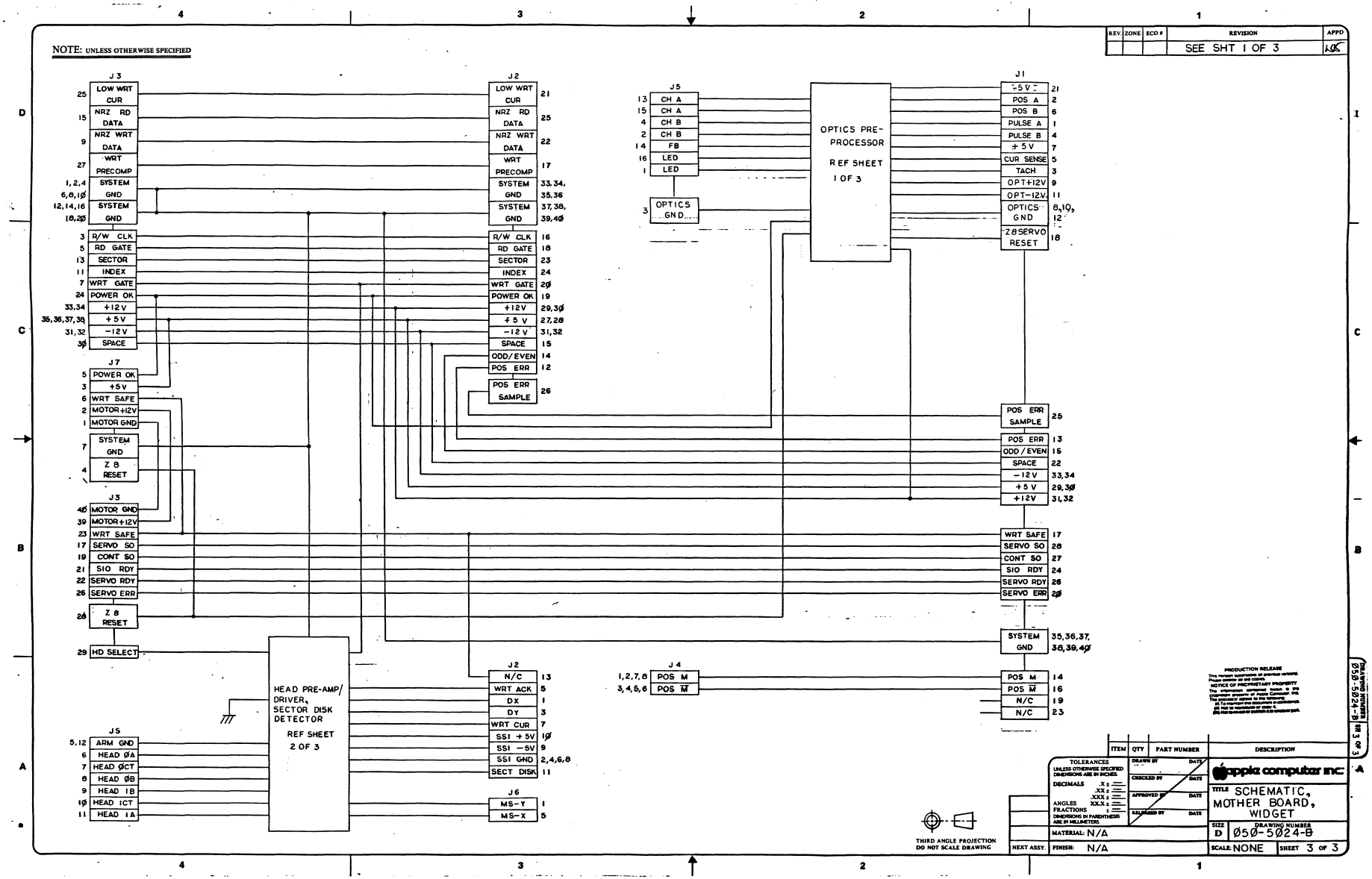
"APPLE_050-5023-B-1of1.PICT" 840 KB 2002-03-12 dpi: 200h x 200v pix: 8516h x 5452v



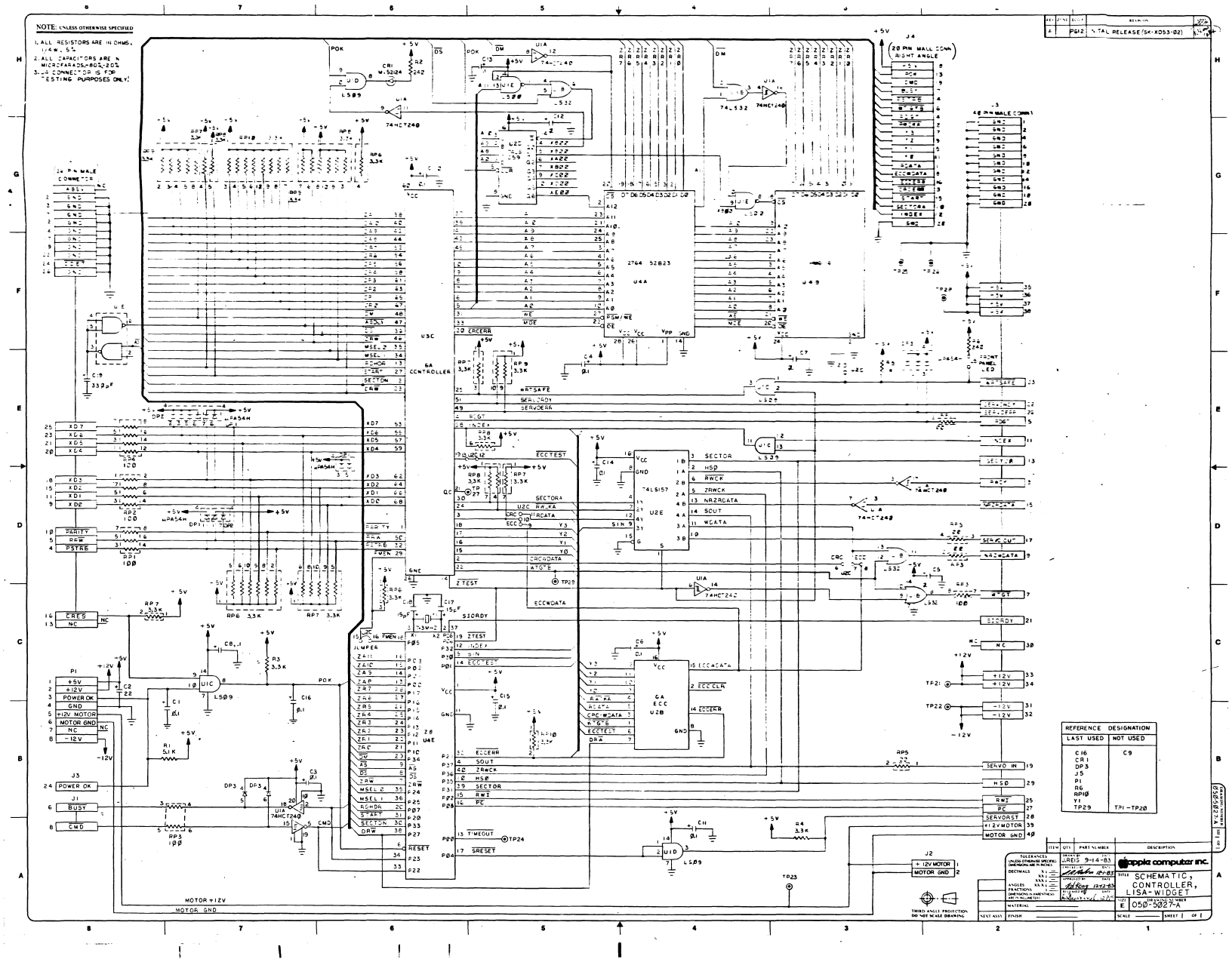
"APPLE_050-5024-B-1of3.PICT" 681 KB 2002-03-12 dpi: 200h x 200v pix: 8680h x 5717v



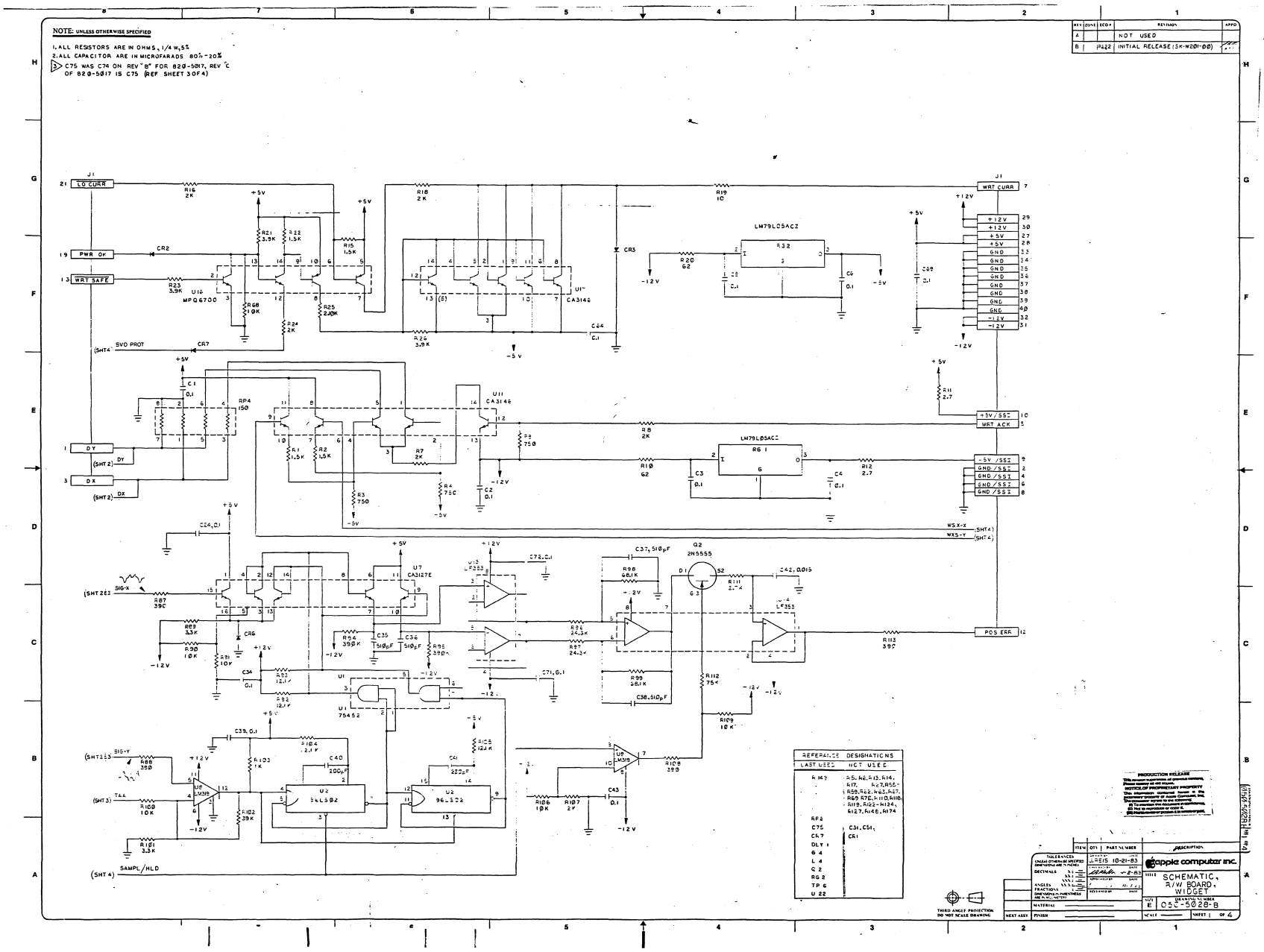
"APPLE_050-5024-B-2of3.PICT" 429 KB 2002-03-12 dpi: 200h x 200v pix: 8709h x 5629v



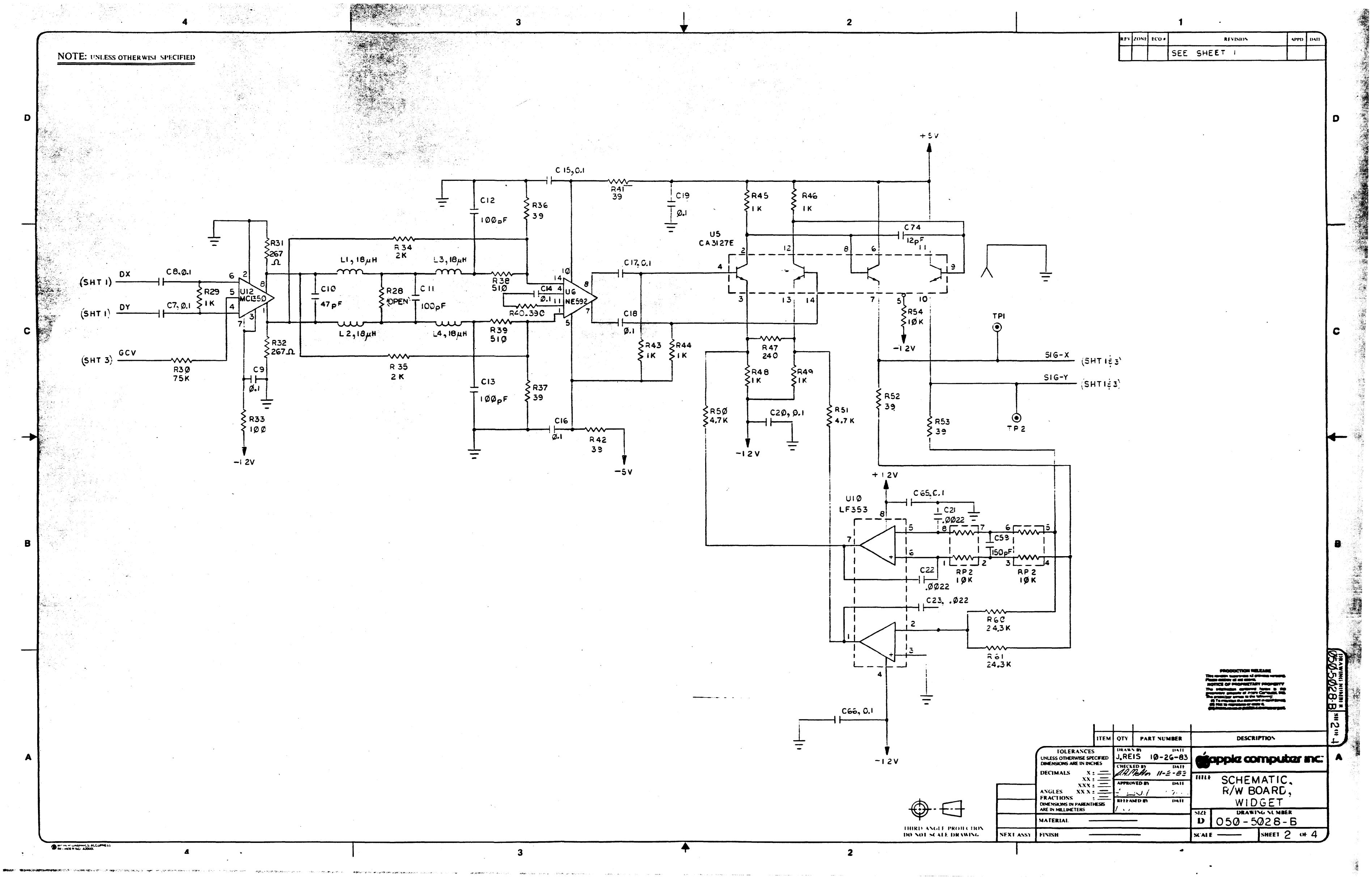
"APPLE_050-5024-B-3of3.PICT" 668 KB 2002-03-12 dpi: 200h x 200v pix: 8741h x 5620v



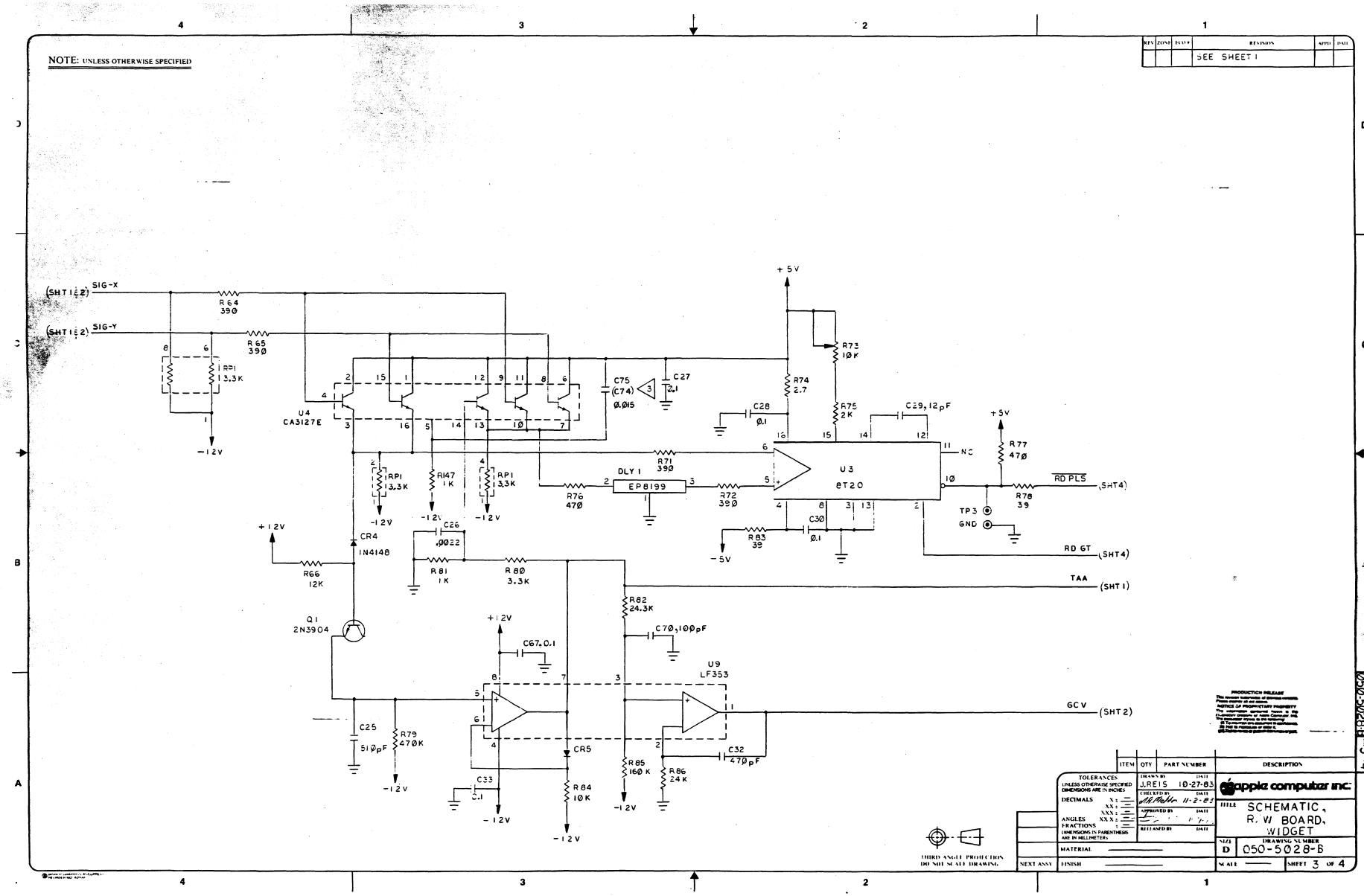
"APPLE_050-5027-A-1of1.PICT" 958 KB 2002-03-12 dpi: 200h x 200v pix: 7893h x 6029v



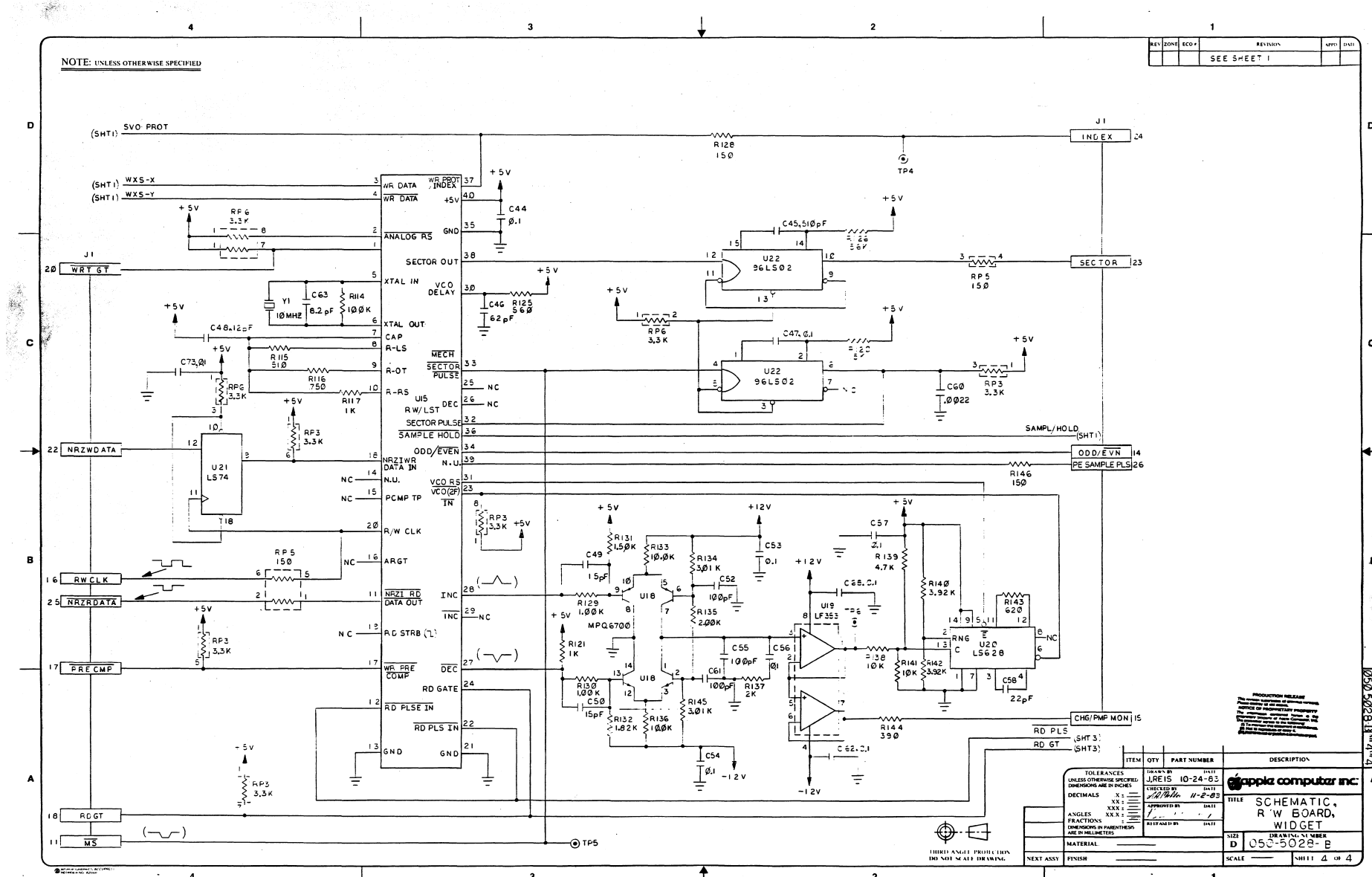
"APPLE_050-5028-B-1of4.PICT" 618 KB 2002-03-12 dpi: 200h x 200v pix: 8071h x 6063v



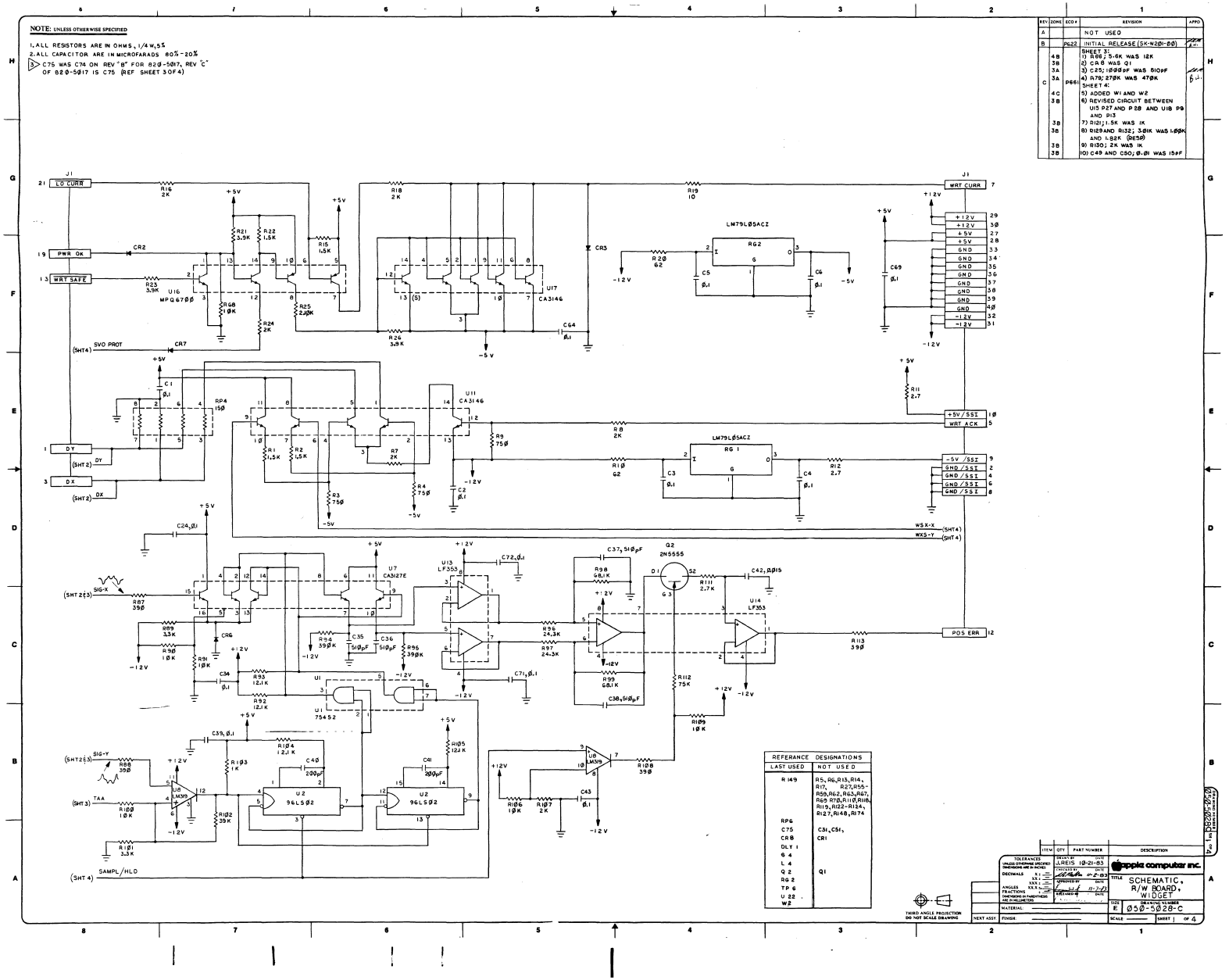
“APPLE_050-5028-B-2of4.PICT” 652 KB 2002-03-12 dpi: 200h x 200v pix: 8682h x 5614v



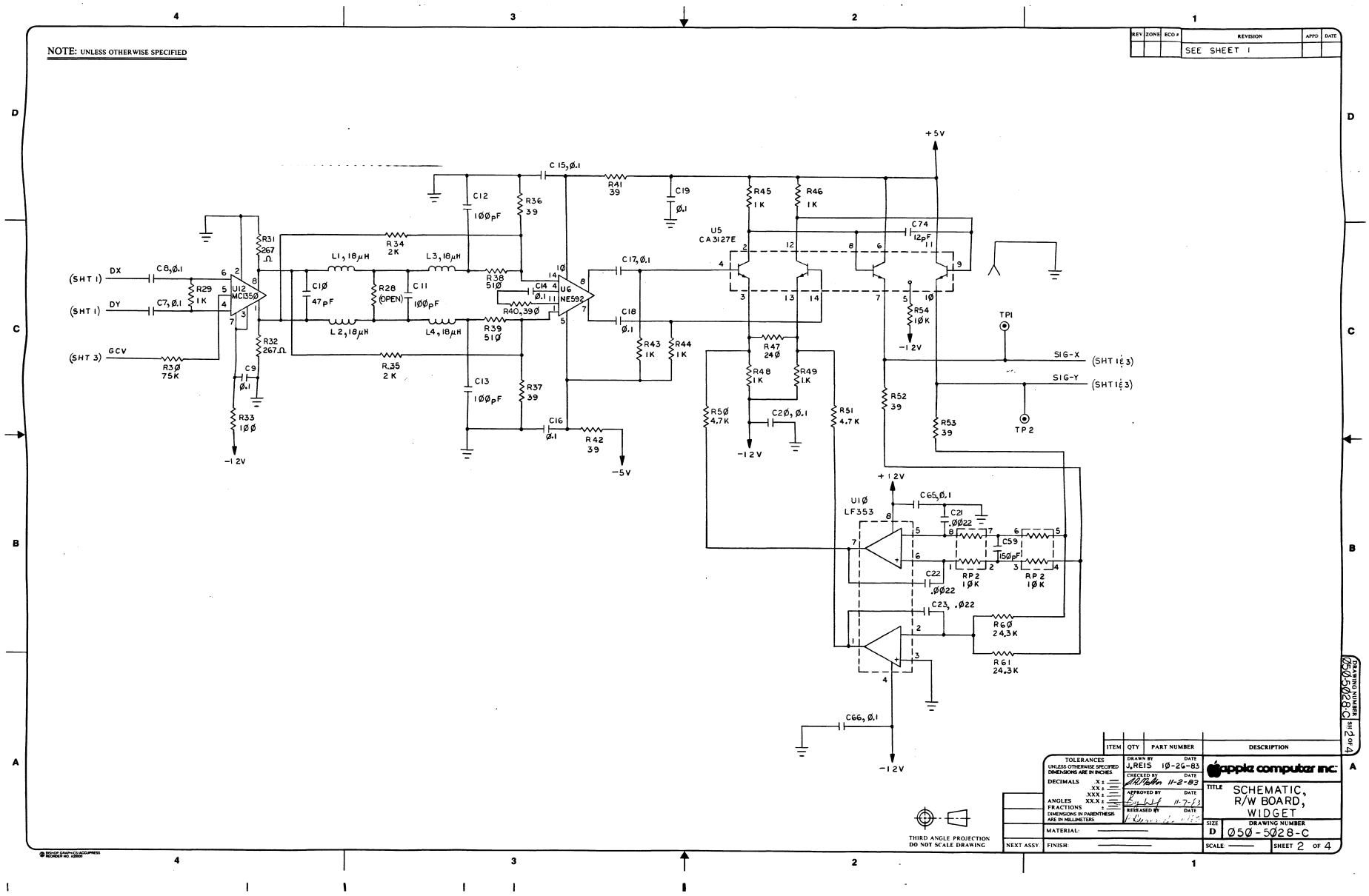
"APPLE_050-5028-B-3of4.PICT" 555 KB 2002-03-12 dpi: 200h x 200v pix: 8670h x 5622v



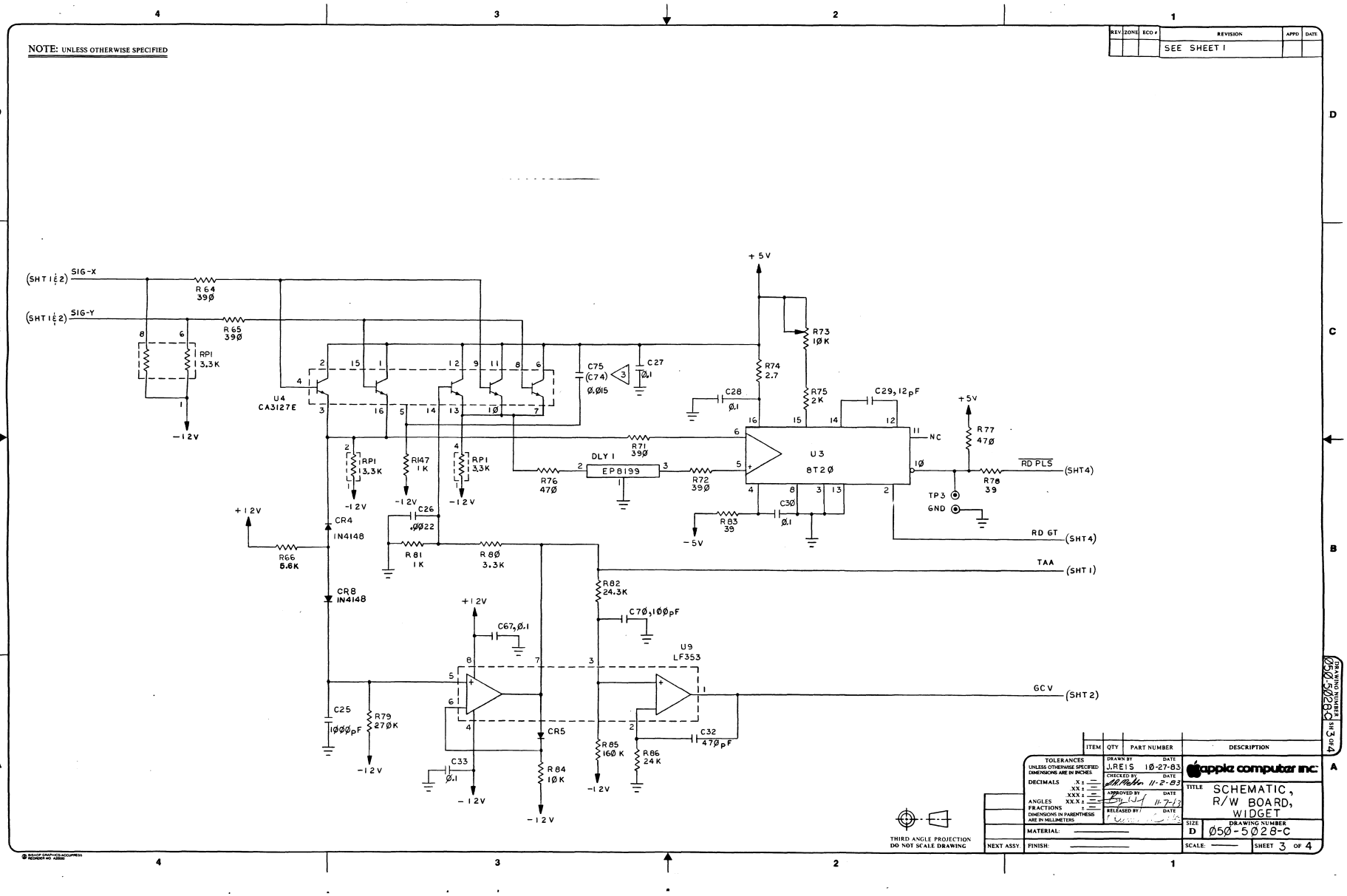
"APPLE_050-5028-B-4of4.PICT" 718 KB 2002-03-12 dpi: 200h x 200v pix: 8711h x 5659v



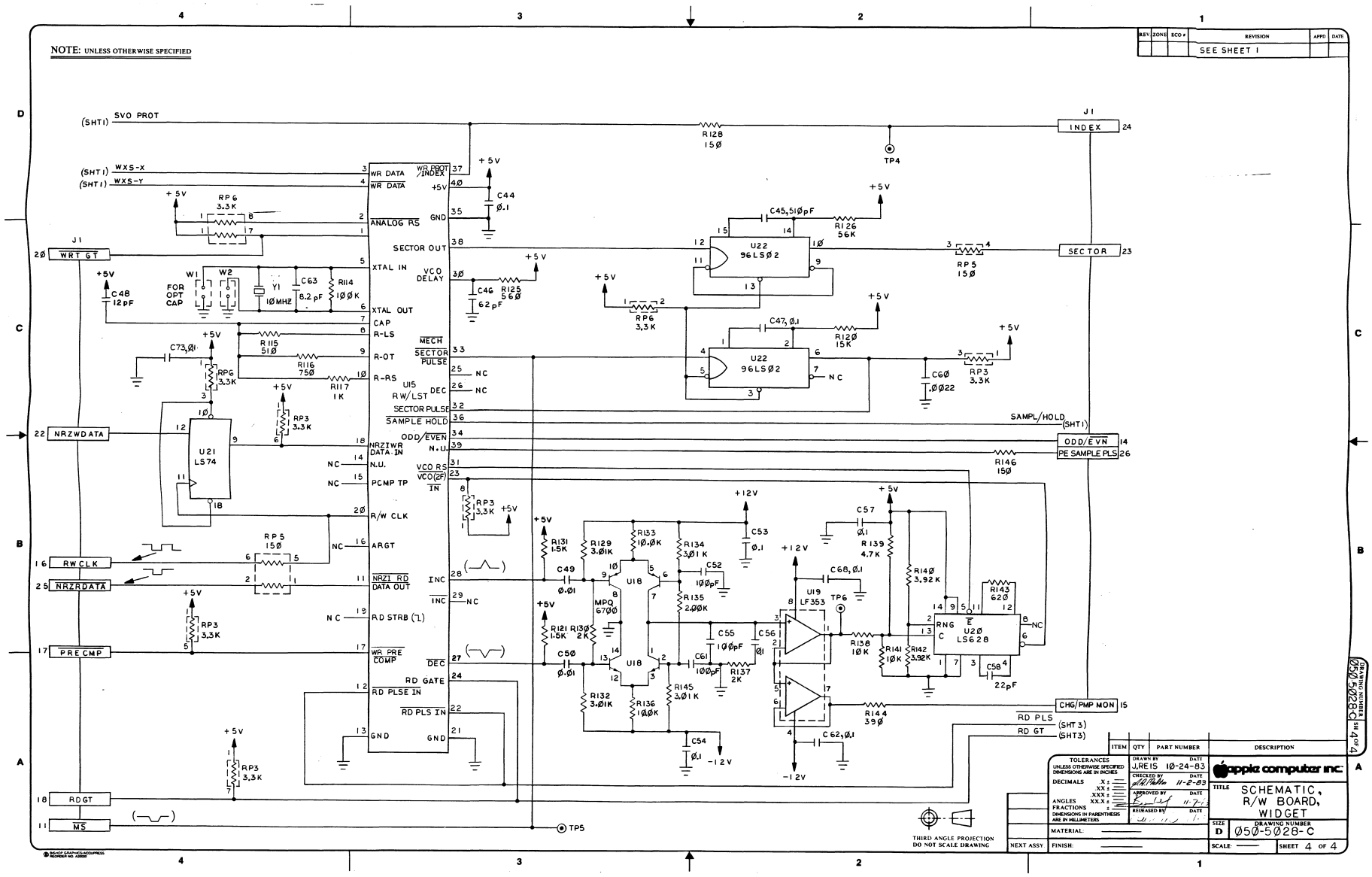
"APPLE_050-5028-C-1of4.PICT" 678 KB 2002-03-12 dpi: 200h x 200v pix: 7835h x 6269v



"APPLE_050-5028-C-2of4.PICT" 498 KB 2002-03-12 dpi: 200h x 200v pix: 8674h x 5642v



"APPLE_050-5028-C-3of4.PICT" 458 KB 2002-03-12 dpi: 200h x 200v pix: 8657h x 5707v

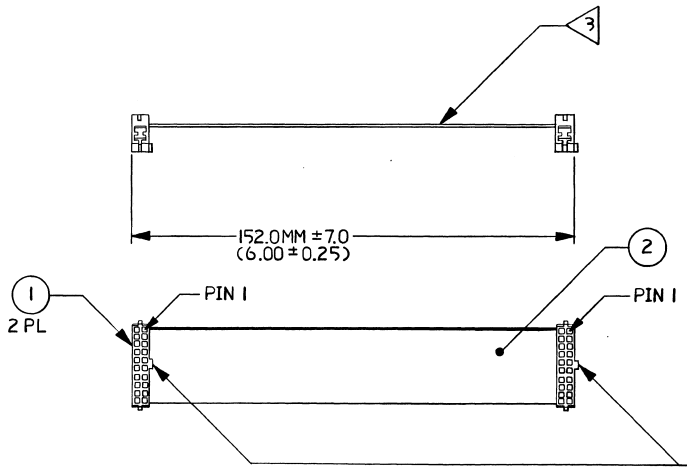


"APPLE_050-5028-C-4of4.PICT" 696 KB 2002-03-12 dpi: 200h x 200v pix: 8800h x 5756v

REV	ZONE	ECO #	REVISION	APPD	DATE
A		F080	INITIAL RELEASE		
A		F207	PRODUCTION RELEASE	[illegible]	8 JAN 84

NOTE: UNLESS OTHERWISE SPECIFIED

1. CABLE ASSEMBLY MUST WITHSTAND 4.5 KG OF FORCE IN ANY DIRECTION WITHOUT ANY DAMAGE TO THE CONNECTORS, ELECTRICAL CONNECTIONS OR CABLE.
2. ELECTRICAL CONNECTIONS OF THE CABLE TO ID CONNECTOR MUST REMAIN GAS TIGHT (150 GRAMS OF CONTACT FORCE) FOR 5 YRS AT 50°C.
3. 20 CONNDUCTOR, 26 GA. STRANDED RIBBON CABLE.



SEE SEPARATE BILL OF MATERIAL: 590-0167

DRAWING NUMBER 590-0167-A SHT 1/1

METRIC

DIMENSIONS ARE IN MILLIMETERS
TOLERANCES
X ± ___ XXX± ___
XX ± ___ ANGLES ± ___
DO NOT SCALE DRAWING

MATERIAL: ___ FINISH: ___

DRFT SQ	5/83	DRFT. CK. L. Bull	6/24/83
ENG APPVL [illegible]	6/24/83	MFG APPVL [illegible]	6/24/83
RELEASE [illegible]	6/8/83	ORIG. DIV MAC	
DESIGNER B.BULL		SCALE FULL	

apple computer inc.

TITLE: ASSY, INTERNAL CABLE, 3 1/2 INCH DRIVE

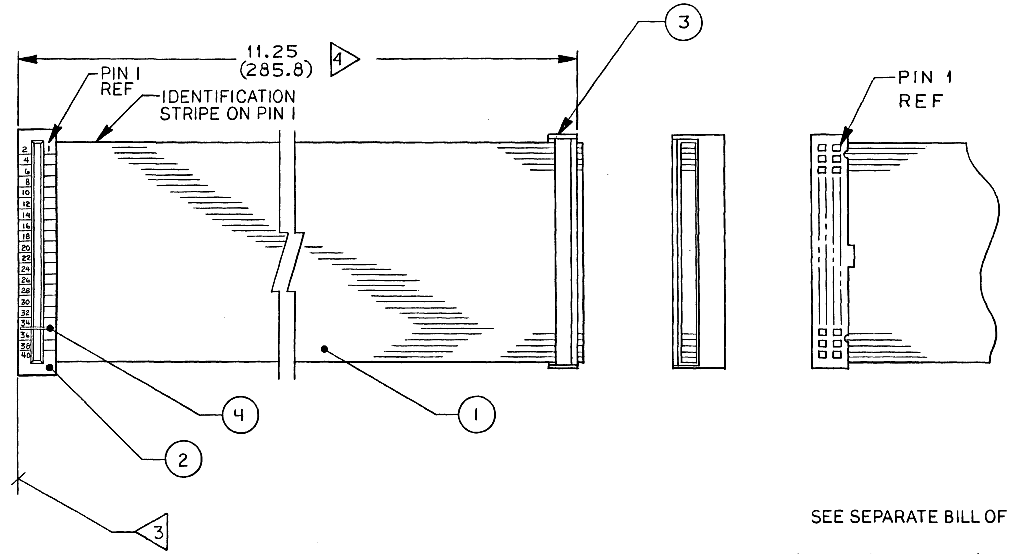
SIZE C | DRAWING NUMBER 590-0167-A | SHT 1/1

"APPLE_590-0167-A-1of1.PICT" 566 KB 2002-03-12 dpi: 200h x 200v pix: 8352h x 6494v

NOTE: UNLESS OTHERWISE SPECIFIED

1. ELECTRICAL CONNECTIONS OF THE ID CONNECTOR MUST REMAIN GAS TIGHT (5.3 OZ OF CONTACT FORCE) FOR 5 YEARS @ 50°C.
2. CABLE MUST WITHSTAND 9.9 LBS OF FORCE IN ANY DIRECTION WITHOUT ANY DAMAGE TO THE CONNECTORS, ELECTRICAL CONNECTIONS OR CABLE.
3. TRIM CABLE FLUSH WITH CONNECTOR HOUSING IN LOCATION SHOWN.
4. INDICATED DIMENSION IS WITH CABLE FULLY EXTENDED.
5. SEE SHEET 2 FOR FOLDED CABLE DETAIL.

REV.	ZONE	ECO #	REVISION	APPD	DATE
A		C626	INITIAL RELEASE		
B	2C 3C 4D	P698	ITEM 3 REVERSED ON ITEM 1 IN ASSY, 11.25 WAS 12.6, ADDED NOTES 4 & 5, ADDED SHEET 2		



SEE SEPARATE BILL OF MATERIALS 590-0207

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± .XX ± .10 .XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY: Shaykа Minasian DATE: 11/83
CHECKED BY: C Swata DATE: 11-12-83
APPROVED BY: Don Ehrlich DATE: 11/83
RELEASED BY DATE

apple computer inc.

TITLE: CABLE ASSEMBLY, MOTHER BOARD – LISA CONTROLLER BOARD

SIZE: C DRAWING NUMBER: 590-0207-B

MATERIAL: SEE BILL OF MATERIALS

FINISH: N/A

NEXT ASSY.

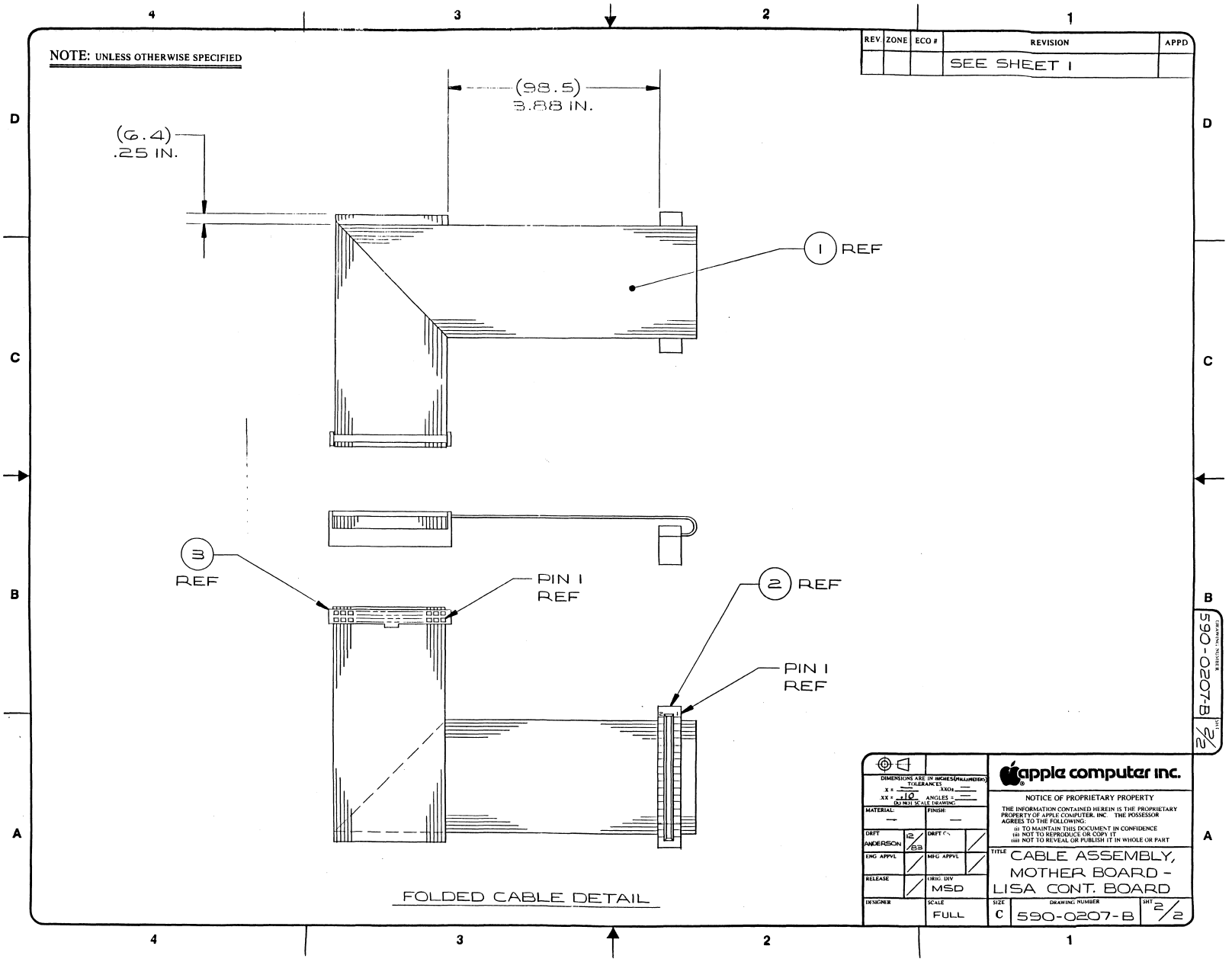
SCALE: NONE SHEET 1 OF 2

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWING NUMBER 590-0207-B SH 1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A10068

"APPLE_590-0207-B-1of2.PICT" 679 KB 2002-03-12 dpi: 200h x 200v pix: 8384h x 6613v



"APPLE_590-0207-B-2of2.PICT" 500 KB 2002-03-12 dpi: 200h x 200v pix: 8292h x 6564v

NOTE: UNLESS OTHERWISE SPECIFIED

1. AFTER WAVE SOLDERING, SECURE BATTERY PACK (ITEM 99) WITH TIE WRAP (ITEM 103).
2. SECURE COMPONENTS Y1, Y2, Y3, L1, AND C12 TO PCB USING RTV (ITEM 105). DO NOT EXPOSE RTV TO WATER OR CLEANING FLUID FOR AT LEAST 24 HRS.
3. THE ASSY REV LEVEL MUST CORRESPOND WITH THE BILL OF MATERIAL REV LEVEL. MANUFACTURING MUST STAMP THE LATEST REV LEVEL IN APPROPRIATE LOCATION ON THE PCB AFTER ASSEMBLY OR REWORK.
4. COMPONENTS NOT LOADED IN THESE POSITIONS.
5. ISOLATE PAD ON D4-1 (CATHODE SIDE), BY CUTTING POWER TRACE ON SOLDER (BACK) SIDE OF PCB. CONNECT D4-1 (CATHODE) TO U7F-10 ON COMPONENT SIDE OF PCB USING #24 AWG KYNAR JUMPER WIRE. SECURE WITH TAK-PAK OR EQUIV.
6. CUT TRACE FROM D5 CATHODE (LEFT SIDE) TO C38 RIGHT SIDE (FAT TRACE FOR +5V).
7. ADD #24 AWG KYNAR JUMPER WIRE FROM D5 CATHODE TO +12V ON FEEDTHROUGH TO THE LEFT OF D7 (NEAR SYMBOL R38). SECURE JUMPER WITH TAK-PAK OR EQUIV.
8. CUT TRACES RP1-13 AND RP1-9. (GRID LOCATION U8B).
9. C13 IS MISSING FROM THE SILKSCREEN. IT IS LOCATED IMMEDIATLEY TO THE RIGHT OF D2 AND ABOVE U14A.
10. C12 DOES NOT HAVE ITS POLARIZATION INDICATED ON THE SILKSCREEN. INSTALL C12 WITH THE POSITIVE TO THE LEFT SIDE.
11. C37 IS MISSING FROM THE SILSCREEN. IT IS LOCATED DIRECTLY ABOVE R36 AND TO THE LEFT OF Y3.
12. ADD A 47pF CAPACITOR (APPLE P/N 131-5701) BETWEEN U4F-6 AND U4F-10. ATTACH THE CAPACITOR DIRECTLY TO THE IC LEG WITH A BEAD OF SOLDER.
13. BLOCK HOLE ON SOLDER SIDE PRIOR TO WAVE SOLDER TO PREVENT CAPACITOR DAMAGE FROM SOLDER FLOW-THROUGH.
14. Y1 MUST BE SECURED SO THAT IT DOES NOT EXTEND INTO "BAR" AREA OUTLINE.
15. ON THE NON-COMPONENT SIDE, CUT THE TRACE AT C33 "+".
16. ADD #24 AWG KYNAR JUMPER WIRE FROM C33 "+" TO THE FEEDTHROUGH NEAR R43.
17. ADD #24 AWG KYNAR JUMPER BETWEEN PINS U7F-11 AND U7F-13 NON-COMPONENT SIDE. LOOP FROM PIN 11 TO PIN 13 MUST BE WIDE ENOUGH TO ALLOW TEST PROBE TO REACH PIN U7F-12 UNOBSTRUCTED.
18. ADD 74LS08 AT LOCATION U1F. 14 PIN IC JUSTIFIED TO BOTTOM HOLES OF 20 PIN HOLE PATTERN.
19. CUT TRACE FROM U6B-6 AT LOCATION BETWEEN PINS U6B-10 & U6B-11, BEFORE FEED THRU.
20. ADD JUMPER WIRES (SIZES 20-40 AWG ACCEPTABLE).
    U1F-14 TO HOLE AT PIN 20 (+5V)
    U1F-2 TO U6B-10
    U1F-3 TO U2C-1
    U1F-1 TO U6B-6
21. NO COMPONENT TO BE STUFFED AT LOCATION R47.

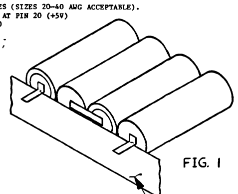
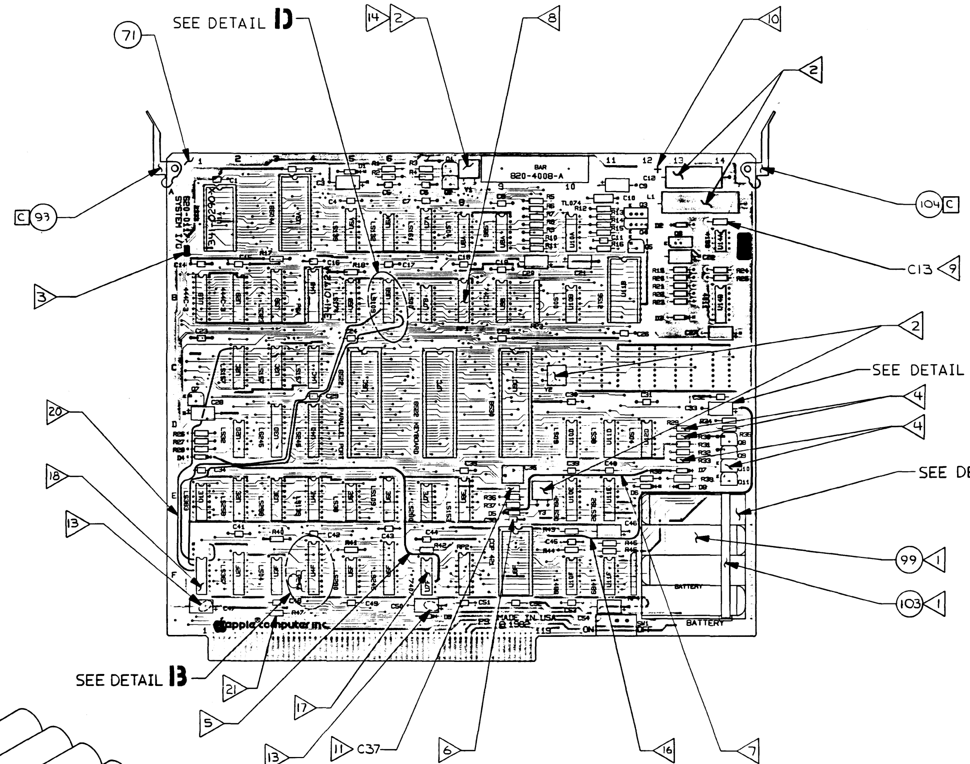


FIG. 1



REV	ZONE	ECO #	REVISION	DATE	APPD
A	—	B083	INITIAL RELEASE	-/82	P.B
B	D4	B096	ADDED NOTES 4—11 CORRECTED NOTE 2	82	PB
C	C1,3	B096	ITEM 104 WAS ITEM 93, ITEM 93 WAS ITEM 104	4/82	[illegible]
D		B116	ADDED DETAIL A, ITEM 106, AND ADDED L1 & C12 TO NOTE 2.	82	PB
E		B116	ADDED NOTE 12 AND DETAIL B.	82	PB
F		B158	ADDED NOTES 13 & 14. NOTES 5 & 7 "TAK-PAK OR EQUIV" WAS RTV.	83	PB
H	—	B181	BOM CHANGE ONLY	2/2	ATN
J	—	B211	ADDED NOTES 15 16 + DETAIL C.	3/83	PB
K	4D 4C	B234	NOTE 5: U7F-10 WAS U7F-12. ADDED NOTE 17. ITEMS 82 & 83 QTY WAS 2.	6/83	UBN
L	—	B303	BOM CHANGE ONLY		PB
M	4C	B338	ADDED NOTES 18, 19 + 20. ADDED DETAIL D	9/7	PB
N	3C	B453	U1A; 341-0290 WAS 341-0138	12/83	T.S. PB
P	3D	B468	ITEM 3 QTY WAS 6. ADDED NOTE 21.	1/84	PB

PRODUCTION RELEASE
This revision supersedes all previous versions.
NOTICE OF PROPRIETARY PROPERTY

PROCEDURE: (PRIOR TO WAVE SOLDER)

1. BEND BOTH TERMINALS OUT AT WELD (FIG. 1).
2. INSERT KAPTON TAPE UNDER TERMINALS, STICKY SIDE TOWARD CELLS (FIG. 1).
3. STICK TAPE TO CELLS AND STRAIGHTEN TERMINALS (FIG. 2).

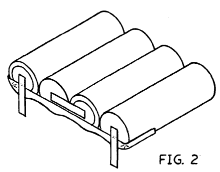
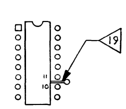
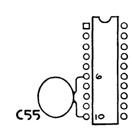


FIG. 2

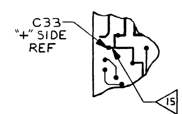
DETAIL A



DETAIL D
SCALE: 2X



DETAIL B
SCALE: 2X



NON-COMPONENT SIDE
DETAIL C

REFERENCE DOCUMENTATION:
SCHEMATIC 050-4008
BILL OF MATERIAL 620-0117

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS X ±, XX ±, XXX ±; ANGLES; FRACTIONS; DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS

DRAWN BY: Ken Jenks 4/16/82
CHECKED BY: Terry Smith 4/?/82
APPROVED BY: P. Baker 4/13/82
RELEASED BY: P. Baker 4/13/82

apple computer inc.

TITLE: ASSEMBLY, PCB SYSTEM I/O LISA

SIZE: D — DRAWING NUMBER: 620-0117-P
MATERIAL: N/A
FINISH: N/A
NEXT ASSY
SCALE: FULL — SHEET 1 OF 1

DRAWING NUMBER 620-0117-P SH 1 OF 1

"APPLE_620-0117-P-1of1.PICT" 1227 KB 2002-03-12 dpi: 200h x 200v pix: 8733h x 5700v

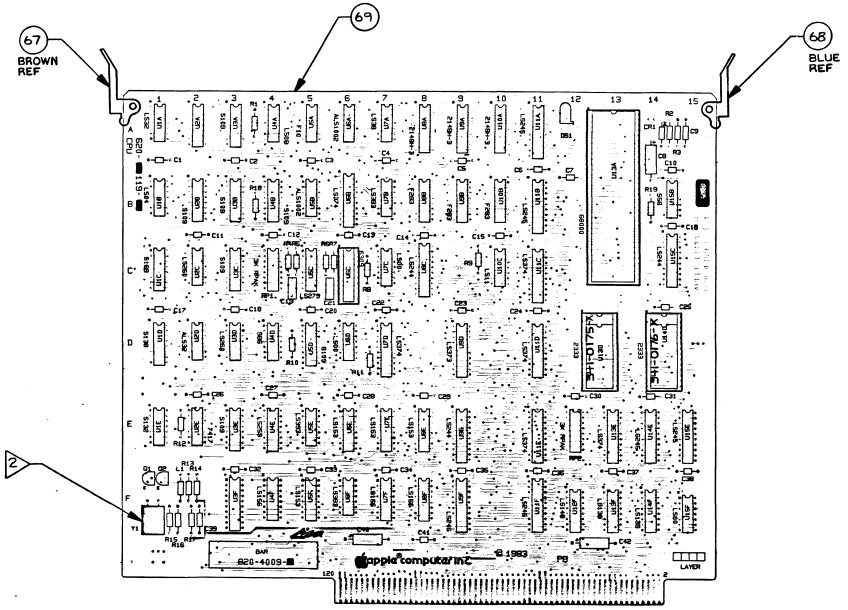
NOTE: UNLESS OTHERWISE SPECIFIED

A ASSY MUST CONFORM TO STANDARDS AS STATED IN APPLE SPEC 060-0012.

A SECURE COMPONENT T1, USING RTV (ITEM 74). DO NOT EXPOSE RTV TO WATER OR CLEANING FLUID FOR AT LEAST 24 HOURS.

3. THE ASSY REV LEVEL MUST CORRESPOND WITH THE BILL OF MATERIAL REV LEVEL. MANUFACTURING MUST STAMP THE LATEST REV LEVEL IN THE APPROPRIATE LOCATION ON THE PCB AFTER ASSEMBLY OR REWORK.

REV	ZONE	ECO #	REVISION	APPD
C	—	B120	REDRAWN: ARTWORK CHANGE	
D	—	B136	U13D WAS 341-0070-C, U14D WAS 341-0071-C, ADDED NOTES 3-6 & DETAIL A	
E	—	B142	U13D WAS 341-0070-D, U14D WAS 341-0071-D	
F	—	B160	ADDED NOTES 7,8 & DETAIL B. U13D WAS 341-0175-A, U14D WAS 341-0176-A	
H	—	B181	BOM CHANGE ONLY	
J	—	B202	REDRAWN: ARTWORK CHANGE DELETED NOTES 3-8 & DETAILS A & B. ADDED R18, R19 & NOTE 1.	KM 7/21/83



COMPONENT VIEW

REFERENCE DOCUMENTATION:
SCHEMATIC 050-4009
BILL OF MATERIAL 620-0119

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS X ± XX ± XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS

DRAWN BY: [illegible] DATE: 6-24-83
CHECKED BY: T. Smith DATE: 7/29/83
APPROVED BY: G. MARTEN DATE: 8/82
RELEASED BY: K. OKIN DATE: 8/82

MATERIAL:
NEXT ASSY. FINISH:

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

apple computer inc.
TITLE: ASSY, PCB, CPU BD LISA
SIZE: D
DRAWING NUMBER: 620-0119-J
SCALE: FULL
SHEET 1 OF 1

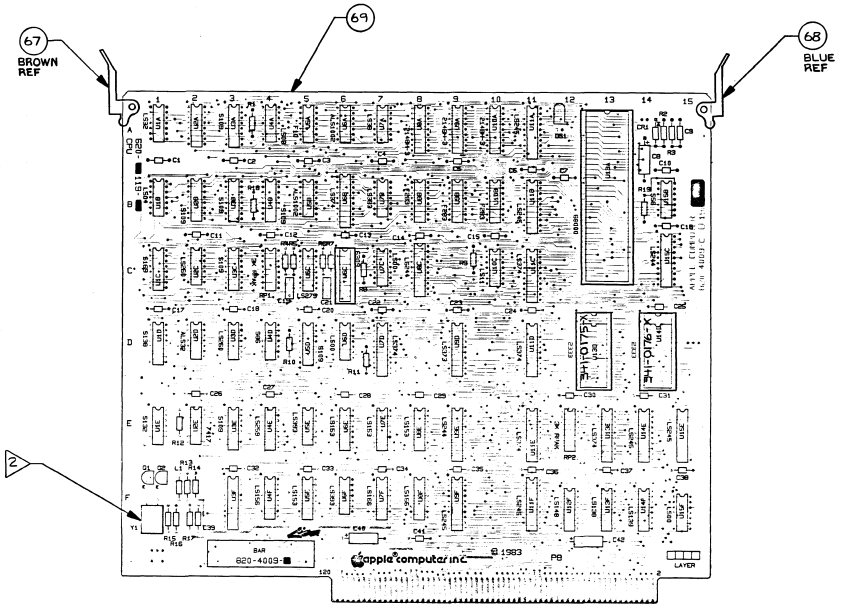
DRAWING NUMBER C-6110-029 SH 1 OF 1

"APPLE_620-0119-J-1of1.PICT" 753 KB 2002-03-12 dpi: 200h x 200v pix: 8686h x 5774v

NOTE: UNLESS OTHERWISE SPECIFIED

1. ASSY MUST CONFORM TO STANDARDS AS STATED IN APPLE SPEC 060-0012.
2. SECURE COMPONENT Y1, USING RTV (ITEM 74). DO NOT EXPOSE RTV TO WATER OR CLEANING FLUID FOR AT LEAST 24 HOURS.
3. THE ASSY REV LEVEL MUST CORRESPOND WITH THE BILL OF MATERIAL REV LEVEL. MANUFACTURING MUST STAMP THE LATEST REV LEVEL IN THE APPROPRIATE LOCATION ON THE PCB AFTER ASSEMBLY OR REWORK.

REV.	ZONE	ECO #	REVISION	APPD
C	—	B120	REDRAWN: ARTWORK CHANGE	
D	—	B136	U13D WAS 341-0070-C, U14D WAS 341-0071-C, ADDED NOTES 3-6 & DETAIL A	
E	—	B142	U13D WAS 341-0070-D, U14D WAS 341-0071-D	
F	—	B160	ADDED NOTES 7,8 & DETAIL B. U13D WAS 341-0175-A, U14D WAS 341-0176-A	
H	—	B181	BOM CHANGE ONLY	
J	—	B202	REDRAWN: ARTWORK CHANGE DELETED NOTES 3-8 & DETAILS A & B. ADDED R18, R19 & NOTE 1.	
K		B404	B.O.M. CHANGE	
L		B466	BOM CHANGE ONLY	



COMPONENT VIEW

REFERENCE DOCUMENTATION:
SCHEMATIC 050-4009
BILL OF MATERIAL 620-0119

PRODUCTION RELEASE

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DECIMALS X ± XX ± XXX ± ANGLES XX ± FRACTIONS ± DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY [illegible] DATE 5-24-85
CHECKED BY T. Smith DATE 7/29/92
APPROVED BY G. MARTEN DATE 8/92
RELEASED BY K. OKIN DATE 8/92

MATERIAL:
NEXT ASSY. FINISH:

apple computer inc

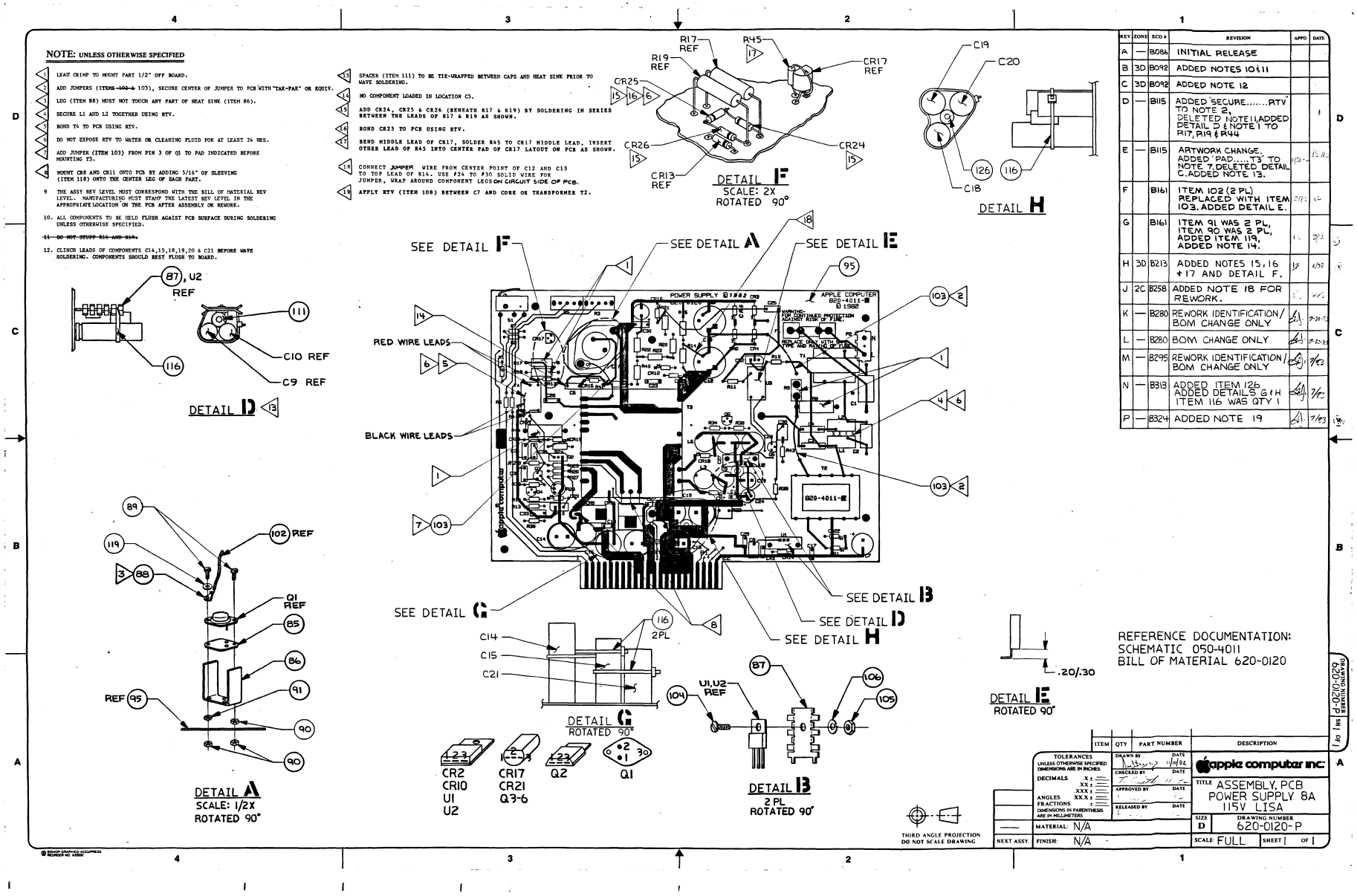
TITLE: ASSY, PCB, CPU BD LISA

SIZE D | DRAWING NUMBER 620-0119-L | SCALE: FULL | SHEET 1 OF 1

DRAWING NUMBER 620-0119-L | SH 1 OF 1

THIRD ANGLE PROJECTION DO NOT SCALE DRAWING

"APPLE_620-0119-L-1of1.PICT" 778 KB 2002-03-12 dpi: 200h x 200v pix: 8714h x 5697v



REV	ZONE	ECO #	REVISION	APPD	DATE
A	—	B086	INITIAL RELEASE		
B	3D	B092	ADDED NOTES 10 & 11		
C	3D	B092	ADDED NOTE 12		
D	—	B115	ADDED 'SECURE.....RTV' TO NOTE 2, DELETED NOTE 11, ADDED DETAIL D & NOTE 1 TO R17, R19 & R44		
E	—	B115	ARTWORK CHANGE. ADDED 'PAD.....T3' TO NOTE 7, DELETED DETAIL C. ADDED NOTE 13.		
F		B161	ITEM 102 (2 PL) REPLACED WITH ITEM 103. ADDED DETAIL E.		
G		B161	ITEM 91 WAS 2 PL, ITEM 90 WAS 2 PL, ADDED ITEM 119, ADDED NOTE 14.		
H	3D	B213	ADDED NOTES 15, 16 + 17 AND DETAIL F.		
J	2C	B258	ADDED NOTE 18 FOR REWORK.		
K	—	B280	REWORK IDENTIFICATION / BOM CHANGE ONLY		
L	—	B280	BOM CHANGE ONLY		
M	—	B295	REWORK IDENTIFICATION / BOM CHANGE ONLY		
N	—	B313	ADDED ITEM 126 ADDED DETAILS G & H ITEM 116 WAS QTY 1		
P	—	B324	ADDED NOTE 19		

ITEM	QTY	PART NUMBER	DESCRIPTION

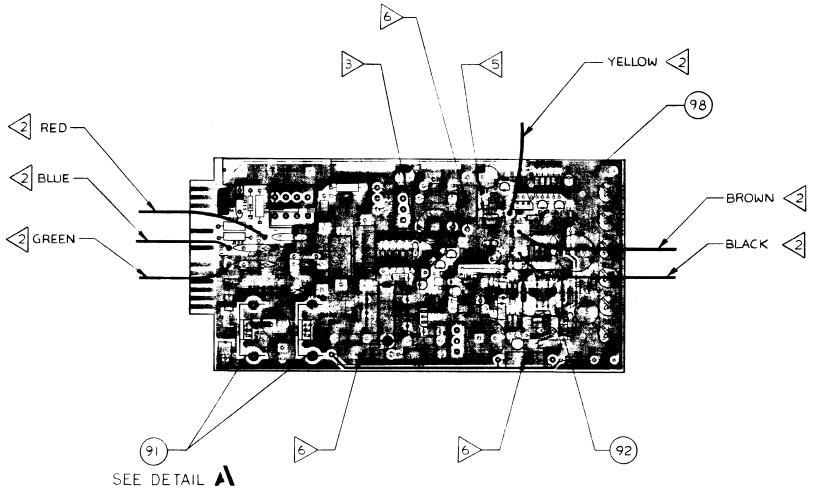
DRAWING NUMBER 620-0120-P SHT 1 OF 1

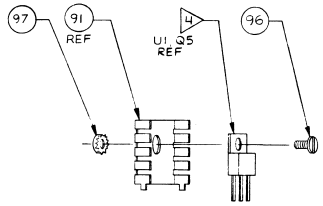
"APPLE_620-0120-P-1of1.PICT" 1151 KB 2002-03-12 dpi: 200h x 200v pix: 8806h x 5827v

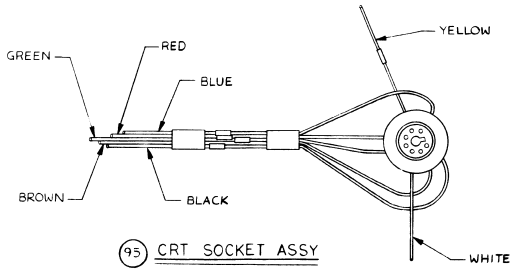
NOTE: UNLESS OTHERWISE SPECIFIED

1. THE ASSY REV LEVEL MUST CORRESPOND WITH THE BILL OF MATERIAL REV LEVEL. MANUFACTURING MUST STAMP THE LATEST REV LEVEL IN THE APPROPRIATE LOCATION ON THE PCB AFTER ASSEMBLY OR REWORK.
2. INDICATED COLORED WIRES ARE THE SAME AS THOSE SHOWN ON CRT SOCKET ASSEMBLY (ITEM 95)
3. DOT TO MATCH DOT ON "L2".
4. U1 AND Q5 BACK SURFACE TO BE COATED WITH HEATSINK COMPOUND BEFORE FASTENING TO HEAT SINK (ITEM 91).
5. L1 TO BE MOUNTED UPRIGHT (PERPENDICULAR TO PCB SURFACE) WITH INDUCTOR PACKAGE EXTENDED OVER L1 SILKSCREEN AREA.
6. R14, R24 & R39 MUST BE MOUNTED 0.100" MIN ABOVE PCB SURFACE.
7. ~~L3 ADJUSTMENT HOLE TO BE FREE OF SOLDER.~~
8. NO COMPONENT TO BE STUFFED AT LOCATION L3.

REV	ZONE	ECO #	REVISION		APPD
A	—	B085	INITIAL RELEASE		—
B	4D	B098	ADDED NOTES 5,6 & 7		
C	—	B156	BOM CHANGE ONLY.		
D	—	B176	BOM CHANGE ONLY		
E	—	B203	BOM CHANGE ONLY.		
F	—	B230	REPLACED P55 WITH [illegible]		
H	4C 4C	B356	DELETED NOTE 7 ADDED NOTE 8, ITEM 4 VALUE WAS 0.05μF U1-L2 WIRE CHANGE DELETED L1 ITEM 33)		







REFERENCE DOCUMENTATION:
SCHEMATIC 050 - 4012
BILL OF MATERIAL 620 - 0121

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS X ± XX ± XXX ±
ANGLES XXX ±
FRACTIONS ±
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS

DRAWN BY R ALLEN 4/24/85 DATE
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

MATERIAL: N/A
FINISH: N/A
NEXT ASSY

apple computer inc.

TITLE ASSEMBLY, PCB, VIDEO BOARD LISA

SIZE D | DRAWING NUMBER 620 - 0121 - H

SCALE: FULL | SHEET 1 OF 1

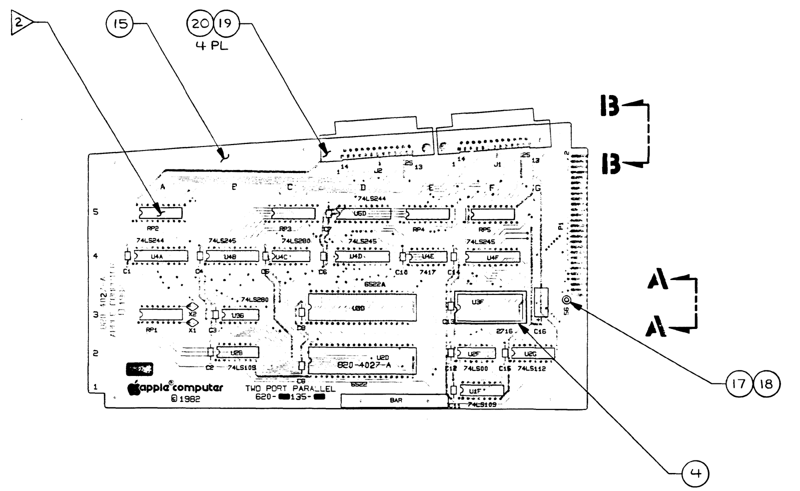
DRAWING NUMBER 620-0121-H SHT 1 OF 1

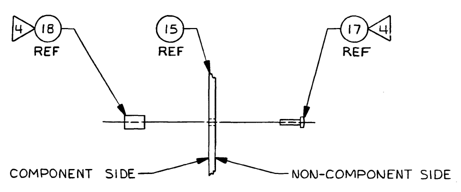
"APPLE_620-0121-H-1of1.PICT" 715 KB 2002-03-12 dpi: 200h x 200v pix: 8597h x 5597v

NOTE: UNLESS OTHERWISE SPECIFIED

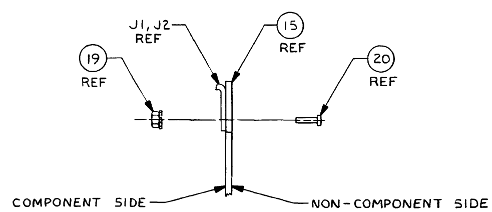
1. THE ASSY REV LEVEL MUST CORRESPOND WITH THE BILL OF MATERIAL REV LEVEL. MANUFACTURING MUST STAMP THE LATEST REV LEVEL IN THE APPROPRIATE LOCATION ON THE PCB AFTER ASSEMBLY OR REWORK.
2. THE 16 PIN R PACKS RP2-RP5 TO BE CENTERED ON 20 PIN PAD LAYOUT. REMAINING 4 HOLES CAN FILL WITH SOLDER.
3. PCB ASSY MUST CONFORM TO APPLE WORKMANSHIP STD 060-0012.
4. APPLY "LOCKTITE" THREADLOCKER #222 TO THREADS OF ITEMS 17 AND 18 BEFORE ASSY.

REV	ZONE	ECO #	REVISION	APP'D
A	—	B178	INITIAL RELEASE	—
B	3C	B250	ITEM 20,4PL WAS ITEM 17,4PL	
B	4D	B467	ADDED NOTE 4.	





VIEW A-A
SCALE: 2X



VIEW B-B
SCALE: 2X
4 PL

REFERENCE DOCUMENTATION:
BILL OF MATERIAL 620-0135
SCHEMATIC 050-4027

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± / .XX ± / .XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS

DRAWN BY Ken Jenks DATE 12/14/82
CHECKED BY T. Smith DATE 4/83
APPROVED BY J. Fitch DATE 4/83
RELEASED BY J. Fitch DATE 4/83

apple computer inc.

TITLE ASSEMBLY, PCB PARALLEL I/F LISA

SIZE D | DRAWING NUMBER 620-0135-B
MATERIAL:
FINISH:
NEXT ASSY
SCALE: FULL | SHEET 1 OF 1

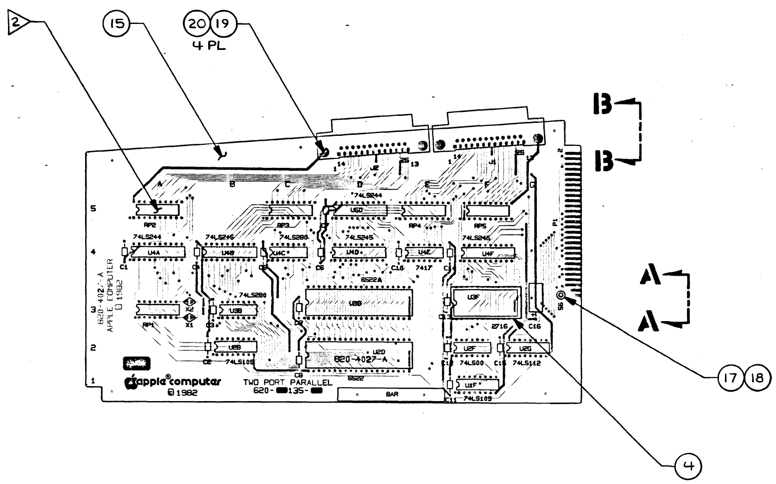
DRAWING NUMBER 620-0135-B SH 1 OF 1

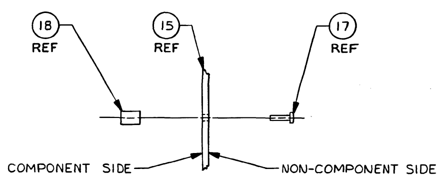
"APPLE_620-0135-B-1of1.PICT" 510 KB 2002-03-12 dpi: 200h x 200v pix: 8655h x 5665v

REV	ZONE	ECO #	REVISION	APPD
A	—	8178	INITIAL RELEASE	—
B	3C	8250	ITEM 20,4PL WAS ITEM 17,4PL	

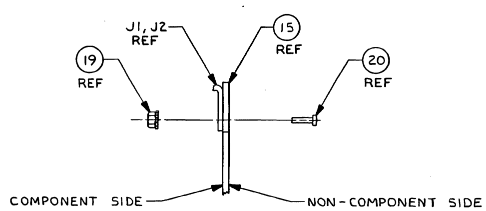
NOTE: UNLESS OTHERWISE SPECIFIED

1. THE ASSY REV LEVEL MUST CORRESPOND WITH THE BILL OF MATERIAL REV LEVEL. MANUFACTURING MUST STAMP THE LATEST REV LEVEL IN THE APPROPRIATE LOCATION ON THE PCB AFTER ASSEMBLY OR REWORK.
2. THE 16 PIN R PACKS RP2-RP5 TO BE CENTERED ON 20 PIN PAD LAYOUT. REMAINING 4 HOLES CAN FILL WITH SOLDER.
3. PCB ASSY MUST CONFORM TO APPLE WORKMANSHIP STD 060-0012.





VIEW A-A
SCALE: 2X



VIEW B-B
SCALE: 2X
4 PL

REFERENCE DOCUMENTATION:
BILL OF MATERIAL 620-0135
SCHEMATIC 050-4027

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± .XX ± .XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Ken Jenks DATE 12/14/82
CHECKED BY T. Smith DATE 1/83
APPROVED BY J. Fidel DATE 4/83
RELEASED BY J. Fidel DATE 4/83

apple computer inc

TITLE ASSEMBLY, PCB PARALLEL I/F LISA

SIZE D
DRAWING NUMBER 620-0135-B
MATERIAL:
NEXT ASSY.
FINISH:
SCALE: FULL SHEET 1 OF 1

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

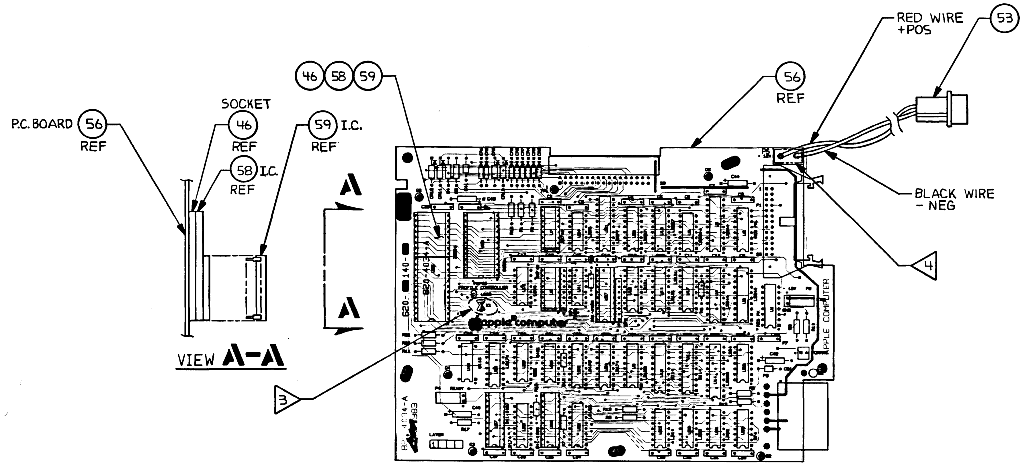
DRAWING NUMBER 620-0135-B SH 1 OF 1

“APPLE_620-0135-B-1of1b.PICT” 570 KB 2002-03-12 dpi: 200h x 200v pix: 8795h x 5726v

REV.	ZONE	ECO #	REVISION	APPD
A	—	B419	INITIAL RELEASE	

NOTE: UNLESS OTHERWISE SPECIFIED

1. ASSY MUST CONFORM TO STANDARDS AS STATED IN APPLE WORKMANSHIP STANDARD 060-0012.
2. THE ASSY REV LEVEL MUST CORRESPOND WITH THE BILL OF MATERIAL REV LEVEL. MANUFACTURING MUST STAMP THE LATEST REV LEVEL IN THE APPROPRIATE LOCATION ON THE PCB AFTER ASSEMBLY OR REWORK.
3. CUT PAD X1 TO COMPLETELY DISCONNECT CIRCUIT.
4. SECURE WIRES TO PCB USING RTV. DO NOT EXPOSE RTV TO WATER OR CLEANING FLUID FOR AT LEAST 24 HRS.



COMPONENT SIDE

REFERENCE DOCUMENTATION:
SCHEMATIC - 050-4034
BILL OF MATERIAL-620-0140

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± — .XX ± — .XXX ± —
ANGLES XX.X ± —
FRACTIONS ± —
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY: [signature] DATE: 11-16-83
CHECKED BY: T. Smith DATE: 11/18/83
APPROVED BY: B. Lee DATE: 12/12/83
RELEASED BY: P. Baker DATE: 12/12/83

apple computer inc

TITLE: ASSEMBLY, PROFILE CONTROLLER, LISA-2.0

SIZE: D — DRAWING NUMBER: 620-0140 -A

MATERIAL: —
FINISH: —
NEXT ASSY. —

SCALE: FULL — SHEET 1 OF 1

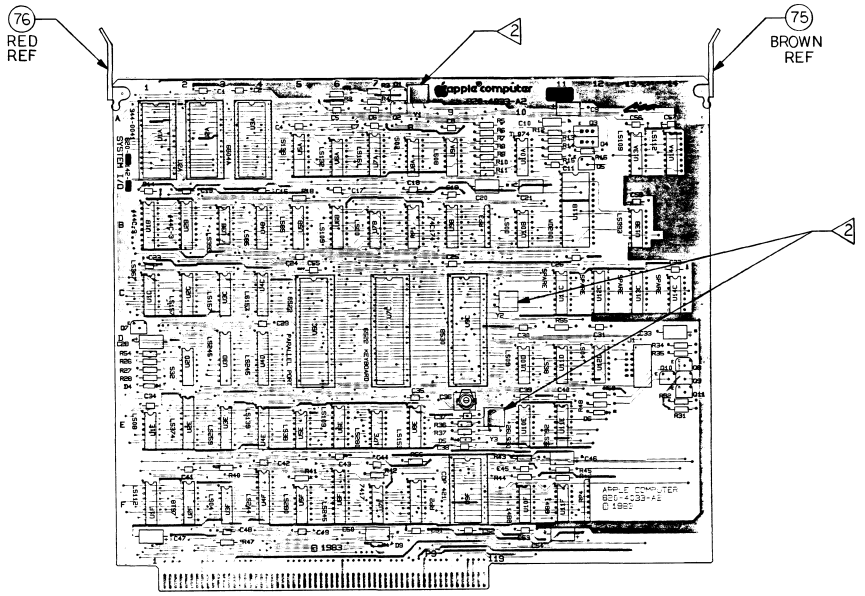
DRAWING NUMBER 620-0140-A SH 1 OF 1

“APPLE_620-0140-A-1of1.PICT” 599 KB 2002-03-12 dpi: 200h x 200v pix: 8473h x 5539v

REV.	ZONE	ECO #	REVISION	APPD
A	—	8335	INITIAL RELEASE	—
B	—	B414	BOM CHANGE	
C	—	B429	BOM CHANGE ONLY	
D	—	B441	BOM CHANGE ONLY	

NOTE: UNLESS OTHERWISE SPECIFIED

1. ASSY MUST CONFORM TO STANDARDS AS STATED IN APPLE SPEC 060-0012.
2. SECURE COMPONENT Y1,Y2 & Y3 USING RTV (ITEM 77). DO NOT EXPOSE RTV TO WATER OR CLEANING FLUID FOR AT LEAST 24 HOURS.
3. THE ASSY REV LEVEL MUST CORRESPOND WITH THE BILL OF MATERIAL REV LEVEL. MANUFACTURING MUST STAMP THE LATEST REV LEVEL IN THE APPROPRIATE LOCATION ON THE PCB AFTER ASSEMBLY OR REWORK.



COMPONENT VIEW

PRODUCTION RELEASE

REFERENCE DOCUMENTATION:
SCHEMATIC 050-4033
BILL OF MATERIAL 620-0142

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS .X ± .XX ± .XXX ±
ANGLES ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS

DRAWN BY S. MINASIAN 9/83
CHECKED BY T. Smith 9/15/83
APPROVED BY Y. Bahn 9/15/83
RELEASED BY Y. Bahn 9/15/83

apple computer inc.

TITLE ASSEMBLY, PCB, I/O BOARD LISA-2.0

MATERIAL: NOTED
FINISH: N/A
NEXT ASSY

SIZE D | DRAWING NUMBER 620-0142-D
SCALE: FULL | SHEET 1 OF 1

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

620-0142-D SHEET 1 OF 1

"APPLE_620-0142-D-1of1.PICT" 764 KB 2002-03-12 dpi: 200h x 200v pix: 8649h x 5590v

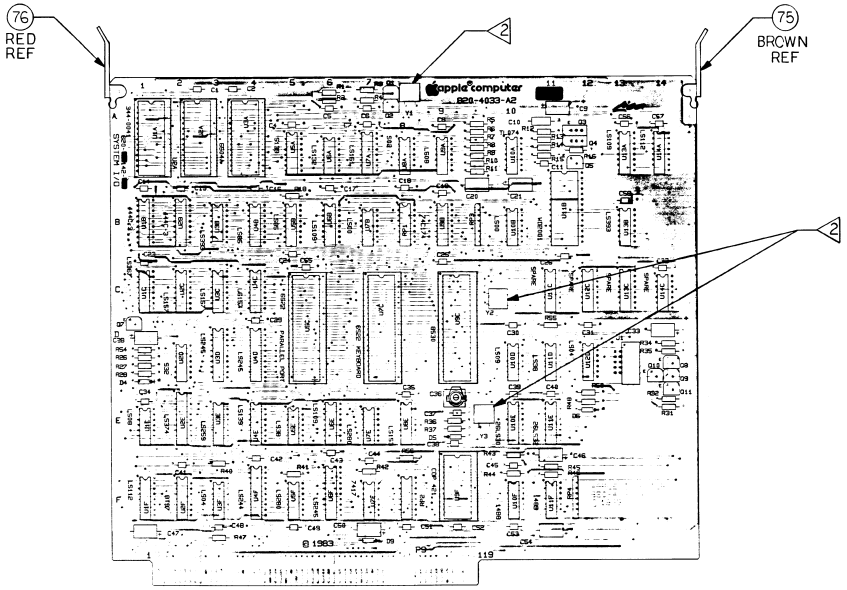
NOTE: UNLESS OTHERWISE SPECIFIED

2. ASSY MUST CONFORM TO STANDARDS AS STATED IN APPLE SPEC 060-0012.

2. SECURE COMPONENT Y1,Y2 & Y3 USING RTV (ITEM 77). DO NOT EXPOSE RTV TO WATER OR CLEANING FLUID FOR AT LEAST 24 HOURS.

3. THE ASSY REV LEVEL MUST CORRESPOND WITH THE BILL OF MATERIAL REV LEVEL. MANUFACTURING MUST STAMP THE LATEST REV LEVEL IN THE APPROPRIATE LOCATION ON THE PCB AFTER ASSEMBLY OR REWORK.

REV	ZONE	ECO #	REVISION	APPD
A	—	B335	INITIAL RELEASE	—
B	—	B414	BOM CHANGE	
C	—	B429	BOM CHANGE ONLY	
D	—	B441	BOM CHANGE ONLY	
E	—	B468	BOM CHANGE ONLY	



COMPONENT VIEW

REFERENCE DOCUMENTATION:
SCHEMATIC 050-4033
BILL OF MATERIAL 620-0142

PRODUCTION RELEASE

NOTICE OF PROPRIETARY PROPERTY

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DECIMALS X ± XX ± XXX ± ANGLES ± FRACTIONS ± DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.	DRAWN BY S. MINASIAN 9/83 CHECKED BY T. Smith 9/15/83 APPROVED BY 9/15/83 RELEASED BY 9/15/83
MATERIAL NOTED	
NEXT ASSY. FINISH: N/A	

apple computer inc.

TITLE ASSEMBLY, PCB, I/O BOARD LISA-2.0

SIZE D | DRAWING NUMBER 620-0142-E

SCALE: FULL | SHEET 1 OF 1

DRAWING NUMBER 620-0142-E SH 1 OF 1

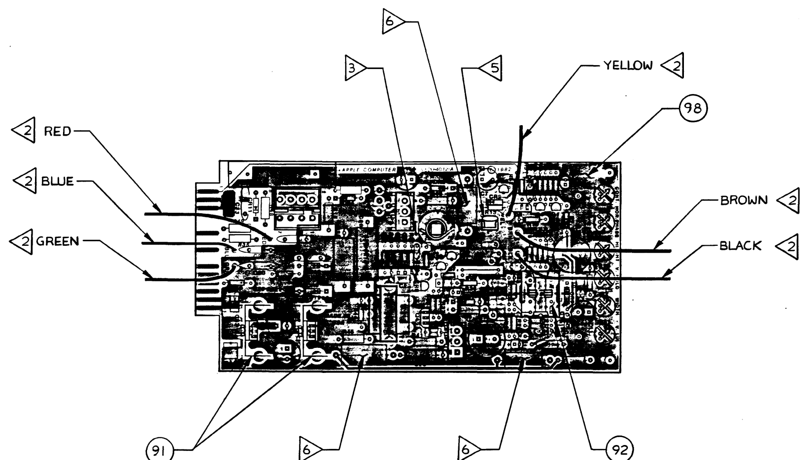
THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

"APPLE_620-0142-E-1of1.PICT" 694 KB 2002-03-12 dpi: 200h x 200v pix: 8726h x 5645v

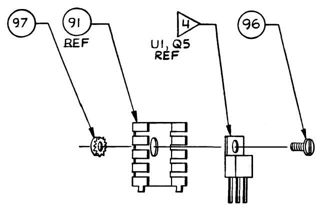
NOTE: UNLESS OTHERWISE SPECIFIED

1. THE ASSY REV LEVEL MUST CORRESPOND WITH THE BILL OF MATERIAL REV LEVEL. MANUFACTURING MUST STAMP THE LATEST REV LEVEL IN THE APPROPRIATE LOCATION ON THE PCB AFTER ASSEMBLY OR REWORK.
2. INDICATED COLORED WIRES ARE THE SAME AS THOSE SHOWN ON CRT SOCKET ASSEMBLY (ITEM 95)
3. DOT TO MATCH DOT ON "L2".
4. U1 AND Q5 BACK SURFACE TO BE COATED WITH HEATSINK COMPOUND BEFORE FASTENING TO HEAT SINK (ITEM 91).
5. L1 TO BE MOUNTED UPRIGHT (PERPENDICULAR TO PCB SURFACE) WITH INDUCTOR PACKAGE EXTENDED OVER L1 SILKSCREEN AREA.
6. R14, R24 & R39 MUST BE MOUNTED 0.100" MIN ABOVE PCB SURFACE.
7. ~~L3 ADJUSTMENT HOLE TO BE FREE OF SOLDER.~~
8. NO COMPONENT TO BE STUFFED AT LOCATIONS: L3, CR6 THRU CR8, C21, C22, R38, R42 & R43.

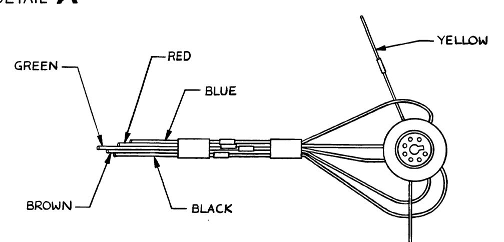
REV.	ZONE	ECO #	REVISION		APPD
A	—	B085	INITIAL RELEASE		—
B	4D	B098	ADDED NOTES 5.6 & 7	23 JUNE 82	
C	—	B156	BOM CHANGE ONLY.		
D	—	B176	BOM CHANGE ONLY		
E	—	B203	BOM CHANGE ONLY.	4/2/83	
F	—	B230	REPLACED R55 WITH CR12; R24 WAS 150 Ω	13 JUNE 1983	G.L.Baker
H	4C 4C	B356	DELETED NOTE 7 ADDED NOTE 8; ITEM 6 VALUE WAS 0.03μF U1 & L2 VALUE CHANGE, DELETED L3 (ITEM 23)	19 OCT 1983	
J	4C 2B	B400	DELETED CR6-8 & CR12; C21 AND C22; R38, R42 AND R43. ADDED R18, R38 & R55. TDA1170N WAS TDA1170.		



SEE DETAIL A



DETAIL A



95 CRT SOCKET ASSY

PRODUCTION RELEASE

REFERENCE DOCUMENTATION:
SCHEMATIC 050-4012
BILL OF MATERIAL 620-0121.

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS .X ± .XX ± .XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS

DRAWN BY R. ALLEN DATE 4/24/82
CHECKED BY T. Smith DATE 4/82
APPROVED BY C.L. BAKER DATE 4/28/82
RELEASED BY P. Baker DATE 5/7/82

apple computer inc.

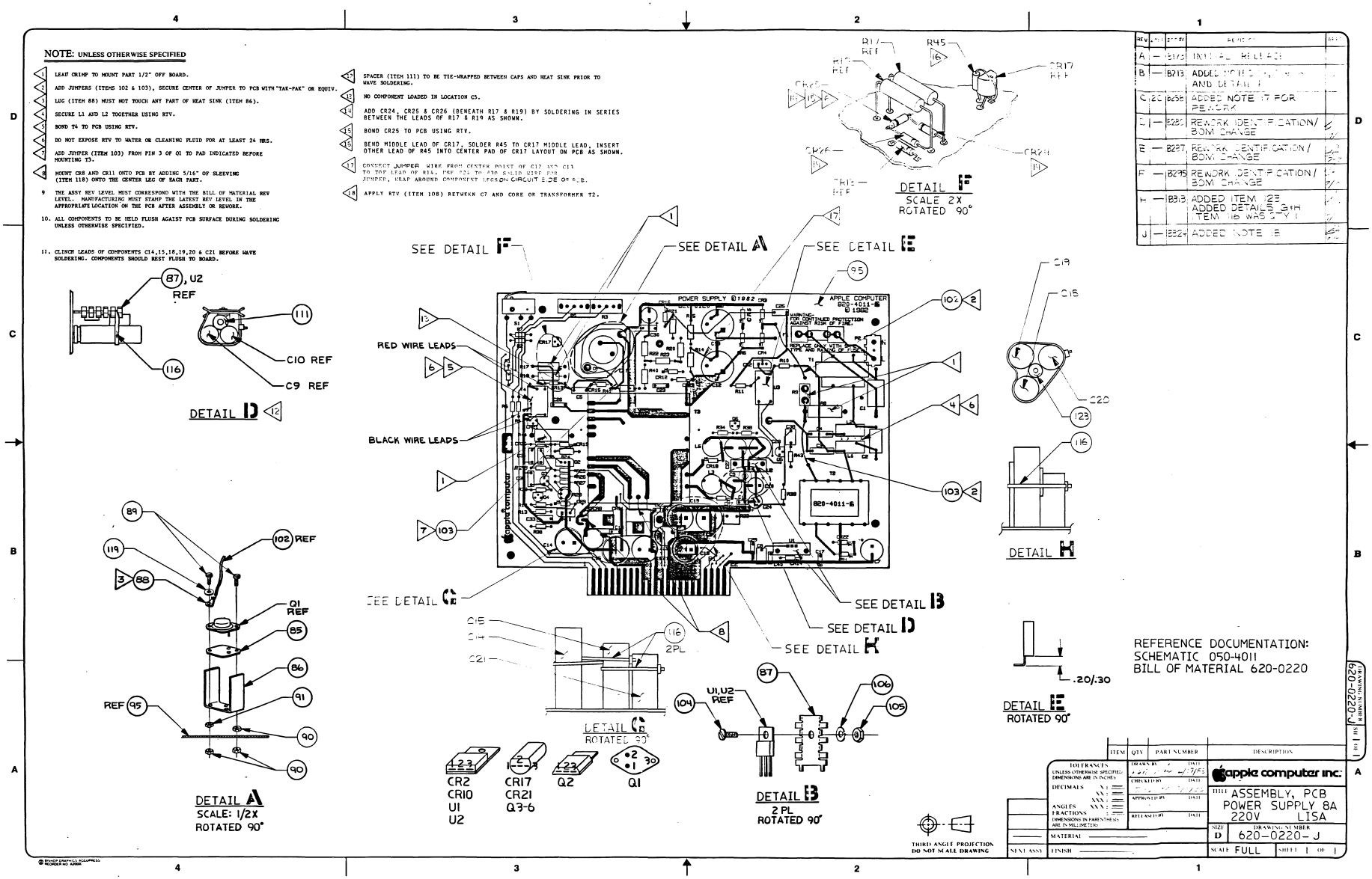
TITLE ASSEMBLY, PCB, VIDEO BOARD LISA

SIZE D DRAWING NUMBER 620-0121-J

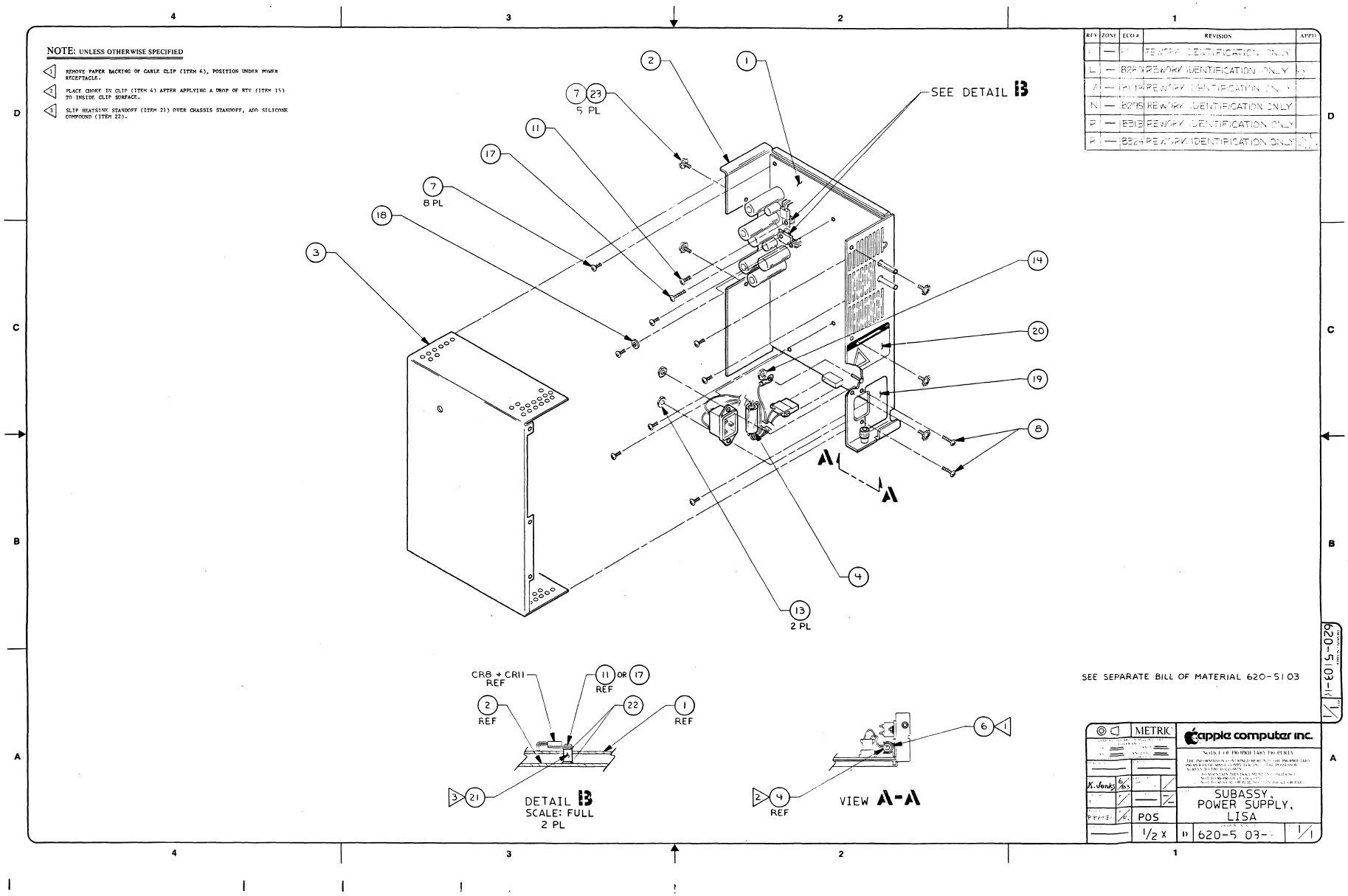
MATERIAL: N/A
NEXT ASSY. FINISH: N/A
SCALE: FULL SHEET 1 OF 1

DRAWING NUMBER 620-0121-J SH 1 OF 1

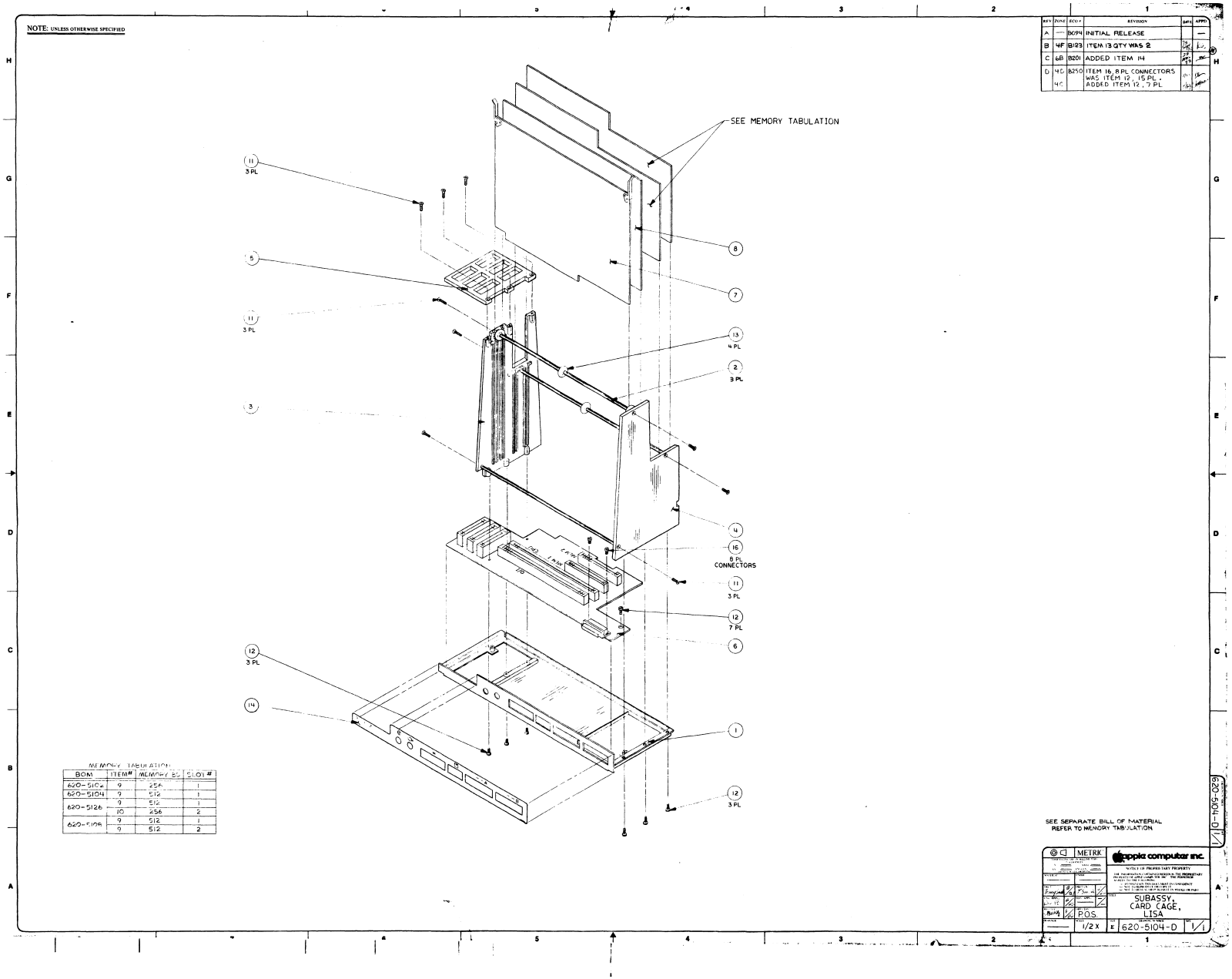
"APPLE_620-0212-J-1of1.PICT" 771 KB 2002-03-12 dpi: 200h x 200v pix: 8699h x 5593v



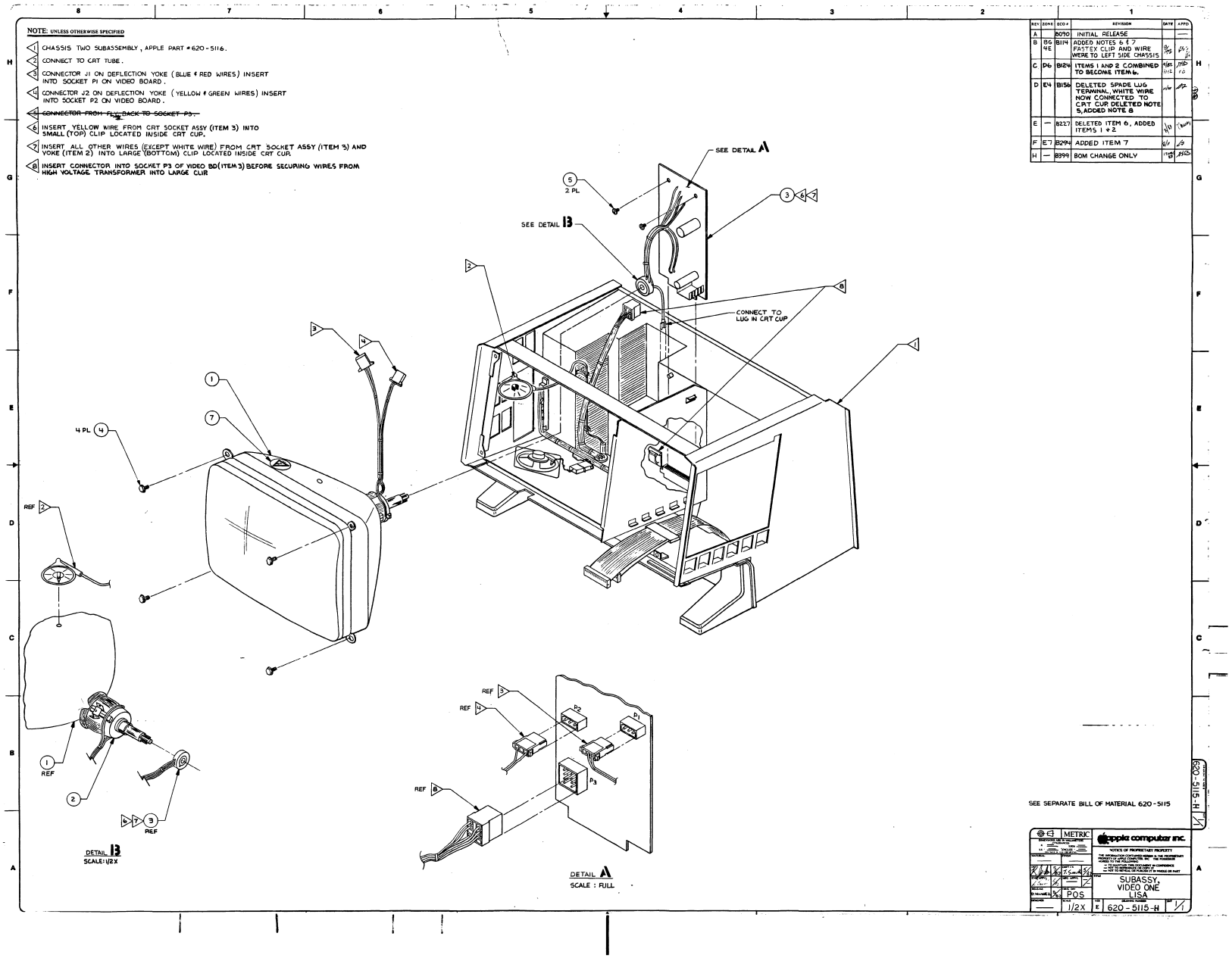
"APPLE_620-0220-J-1of1.PICT" 1006 KB 2002-03-12 dpi: 200h x 200v pix: 8715h x 5639v



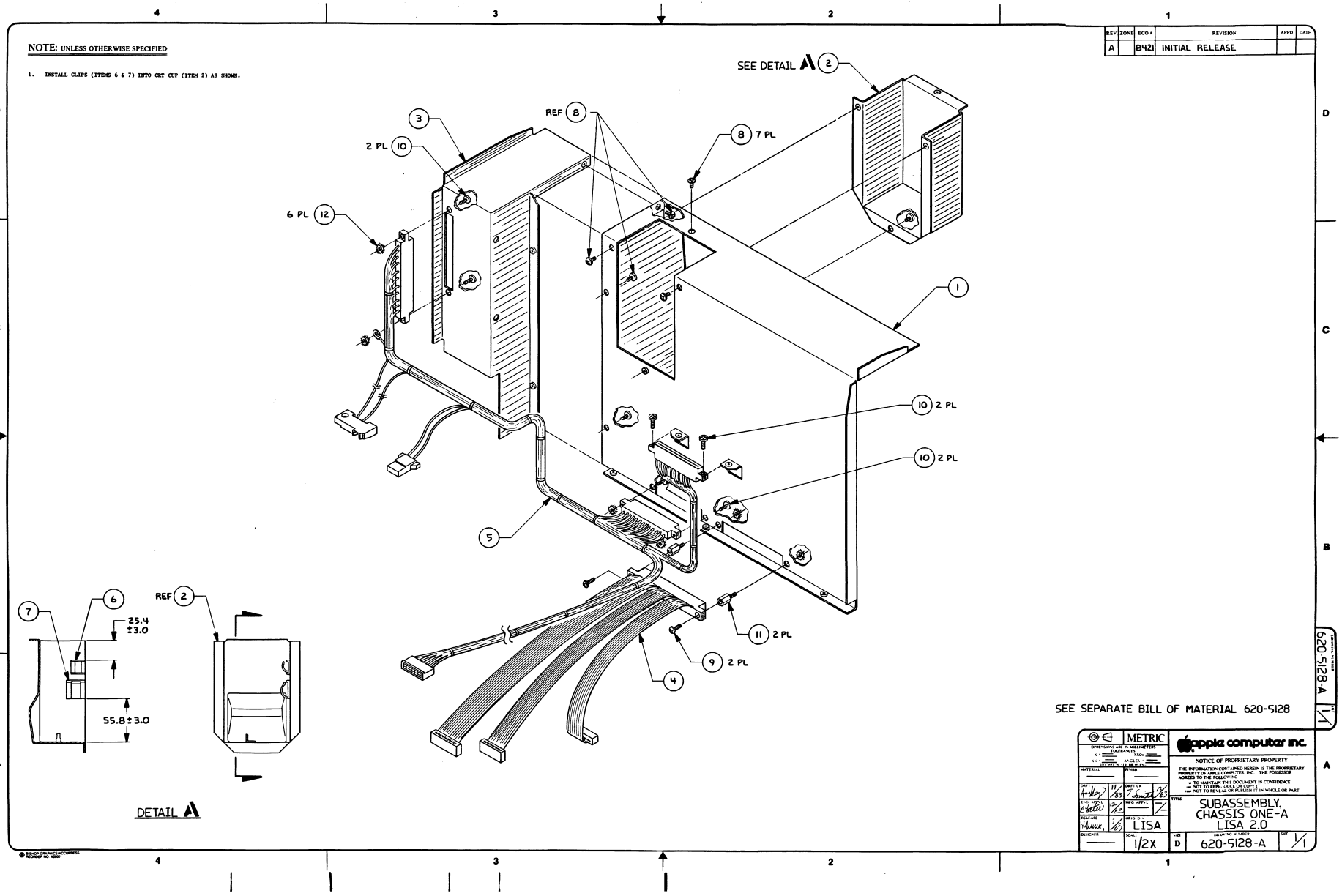
"APPLE_620-5103-R-1of1.PICT" 575 KB 2002-03-12 dpi: 200h x 200v pix: 8786h x 5738v



"APPLE_620-5104-D-1of1.PICT" 651 KB 2002-03-12 dpi: 200h x 200v pix: 9132h x 7094v



"APPLE_620-5115-H-1of1.PICT" 725 KB 2002-03-12 dpi: 200h x 200v pix: 8022h x 6221v


NOTE: UNLESS OTHERWISE SPECIFIED
1. INSTALL CLIPS (ITEMS 6 & 7) INTO CRT CUP (ITEM 2) AS SHOWN.
REV | ZONE | ECO # | REVISION | APPD | DATE
A | | B421 | INITIAL RELEASE | |
SEE DETAIL A
2
3
REF 8
8 7 PL
2 PL 10
6 PL 12
1
10 2 PL
10 2 PL
5
11 2 PL
9 2 PL
4
7
6
25.4 ±3.0
55.8±3.0
REF 2
DETAIL A
SEE SEPARATE BILL OF MATERIAL 620-5128
620-5128-A
METRIC
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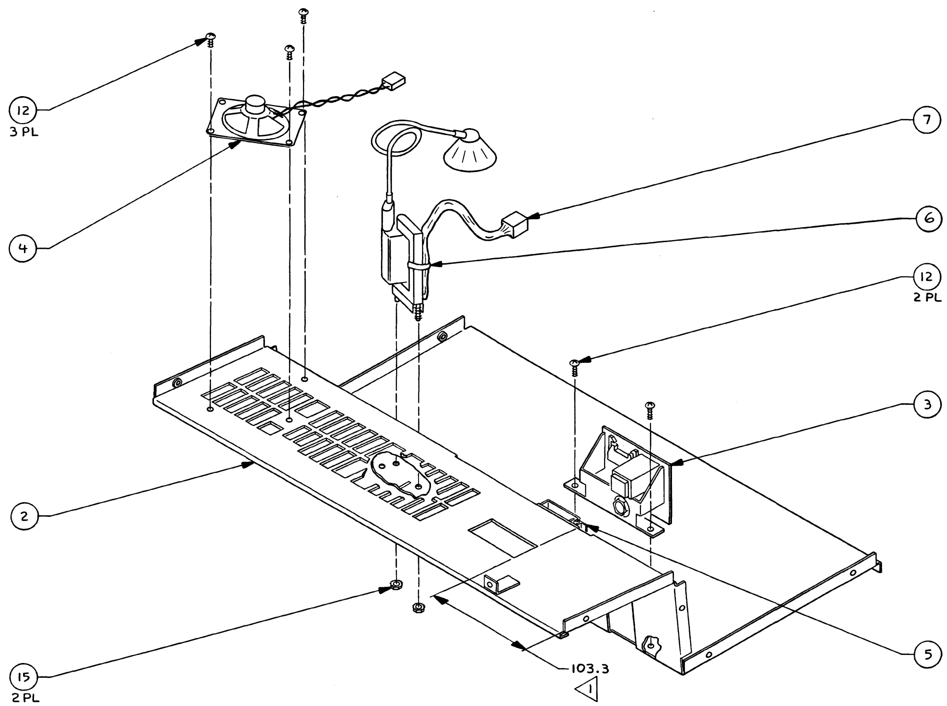
TITLE
SUBASSEMBLY, CHASSIS ONE-A LISA 2.0
LISA
1/2X
D
620-5128-A
1/1

REV	ZONE	ECO #	REVISION	APPD	DATE
A	—	B422	INITIAL RELEASE		

NOTE: UNLESS OTHERWISE SPECIFIED

1. ADHERE DEK CLAMP (ITEM 5) TO CHASSIS (ITEM 2) PER DIMENSION.
2. ROUTE CABLES THROUGH DEK CLAMP (ITEM 5).
3. SECURE TIE-WRAP (ITEM 6) TO FIFTH CHASSIS SLOT FROM PEM.



SEE SEPARATE BILL OF MATERIAL 620-5129

METRIC

DIMENSIONS ARE IN MILLIMETERS
TOLERANCES
X = ___ XXO± ___
XX = ___ ANGLES ± ___
DO NOT SCALE DRAWING

MATERIAL	FINISH
—	—

DRFT		DRFT CK	
K Jenks	12/6/83	T. Smith	12/83
ENG APPVL: E. Vetter	12/83	MFG APPVL: —	—
RELEASE: Terry Smith	12/83	ORIG DIV: LISA	
DESIGNER: —		SCALE: 1/2X	

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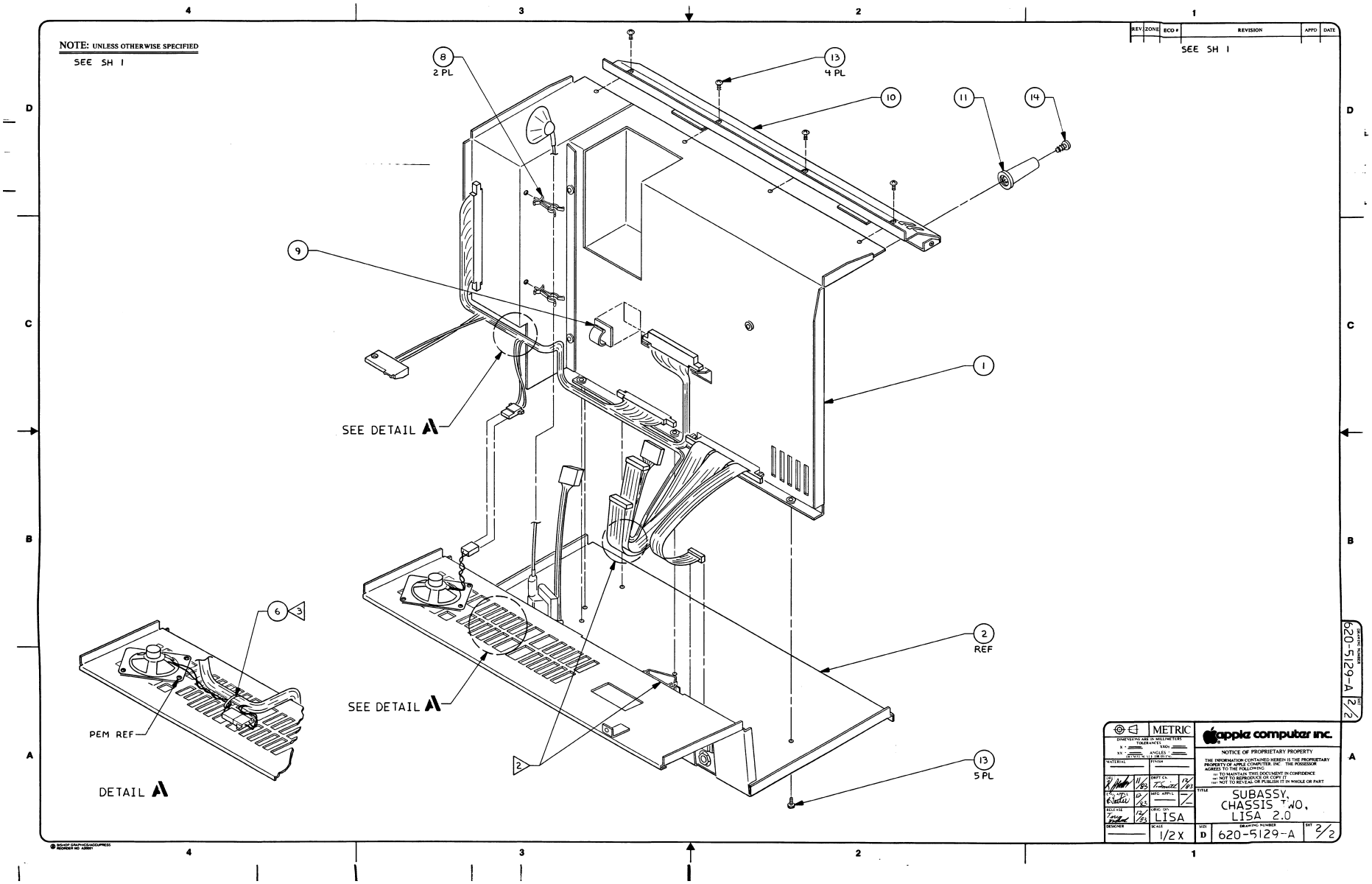
(iii) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

TITLE: SUBASSY, CHASSIS TWO, LISA 2.0

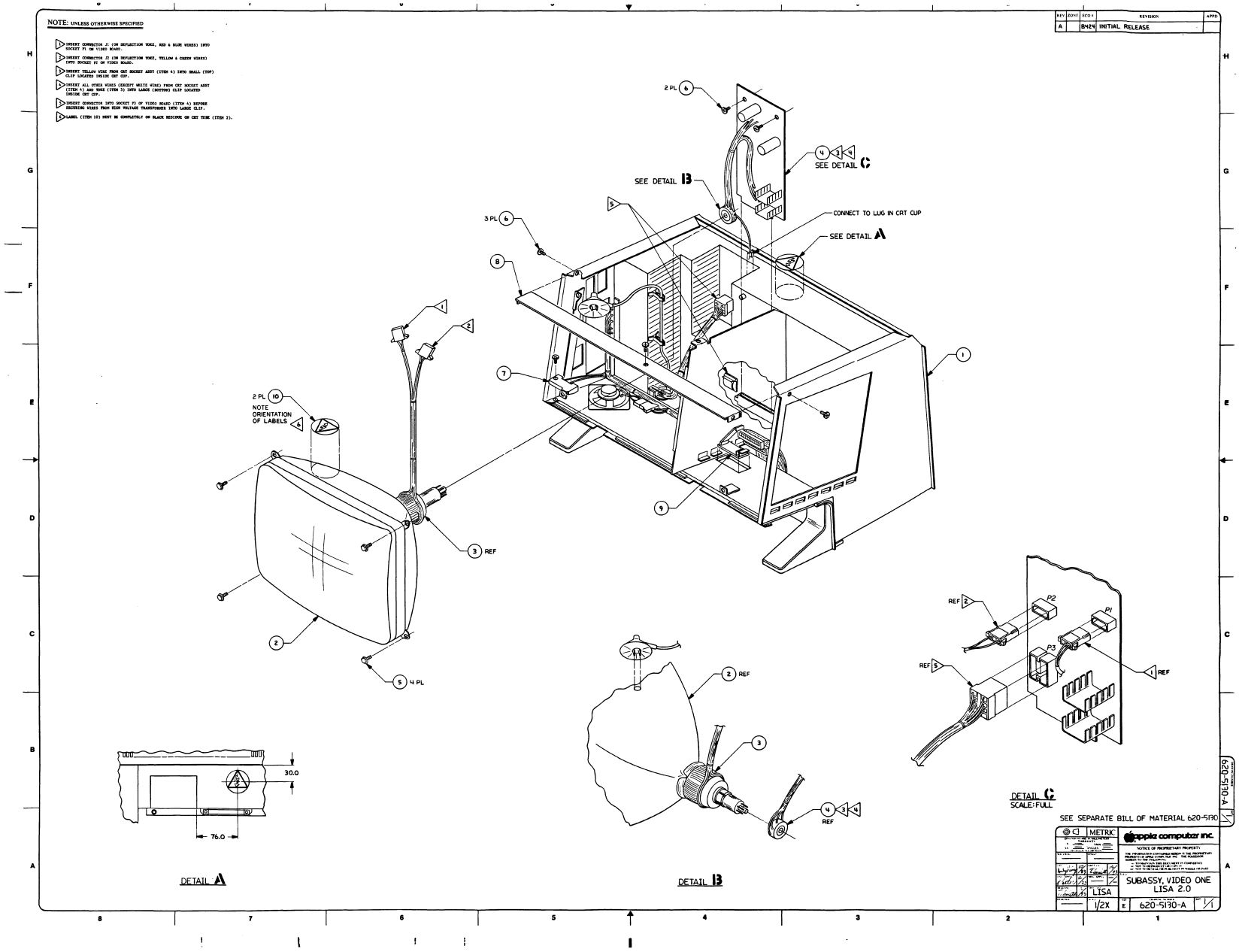
SIZE	DRAWING NUMBER	SHT
D	620-5129-A	1/2

620-5129-A 1/2

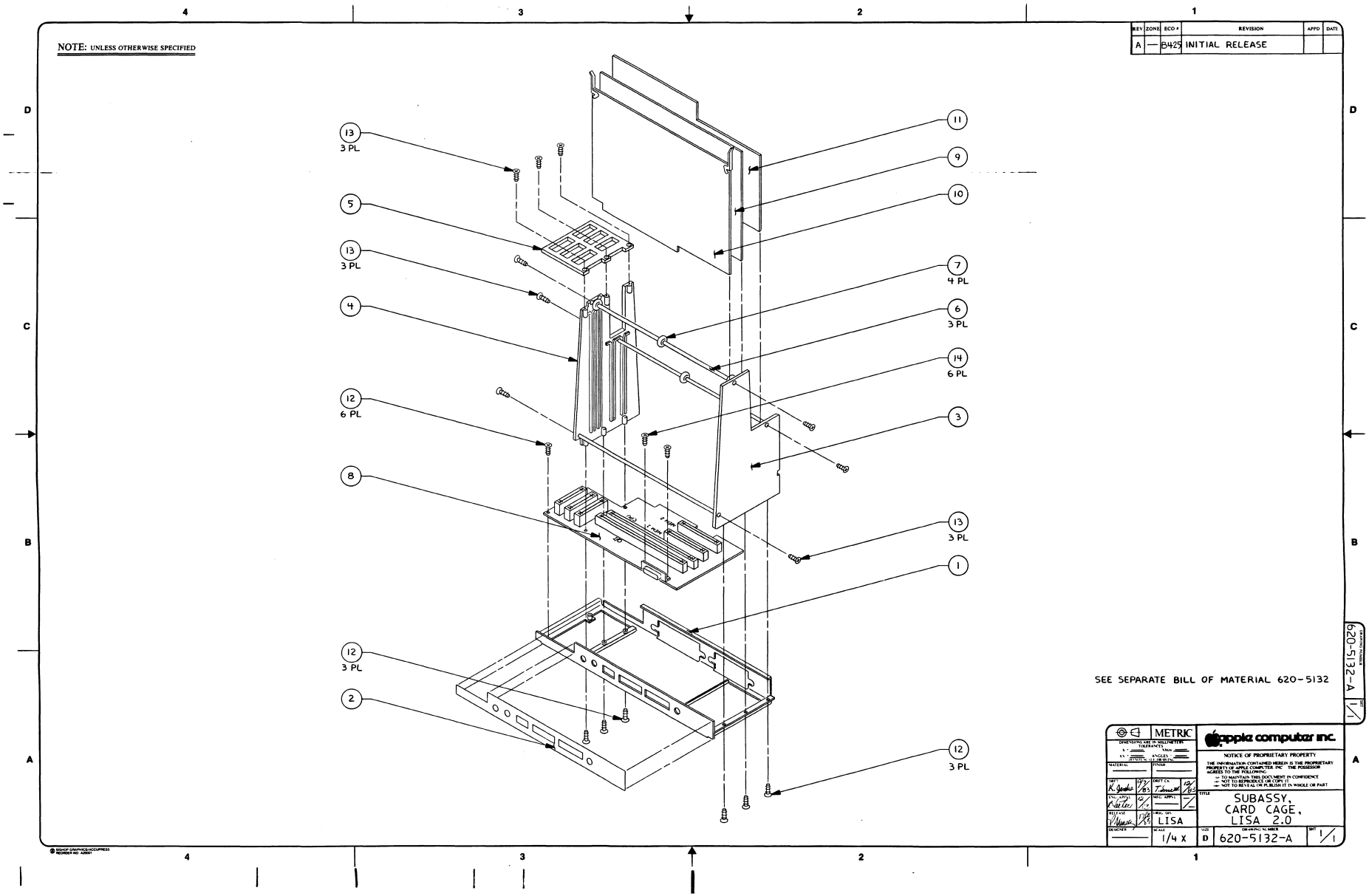
“APPLE_620-5129-A-1of2.PICT” 454 KB 2002-03-12 dpi: 200h x 200v pix: 8641h x 5668v



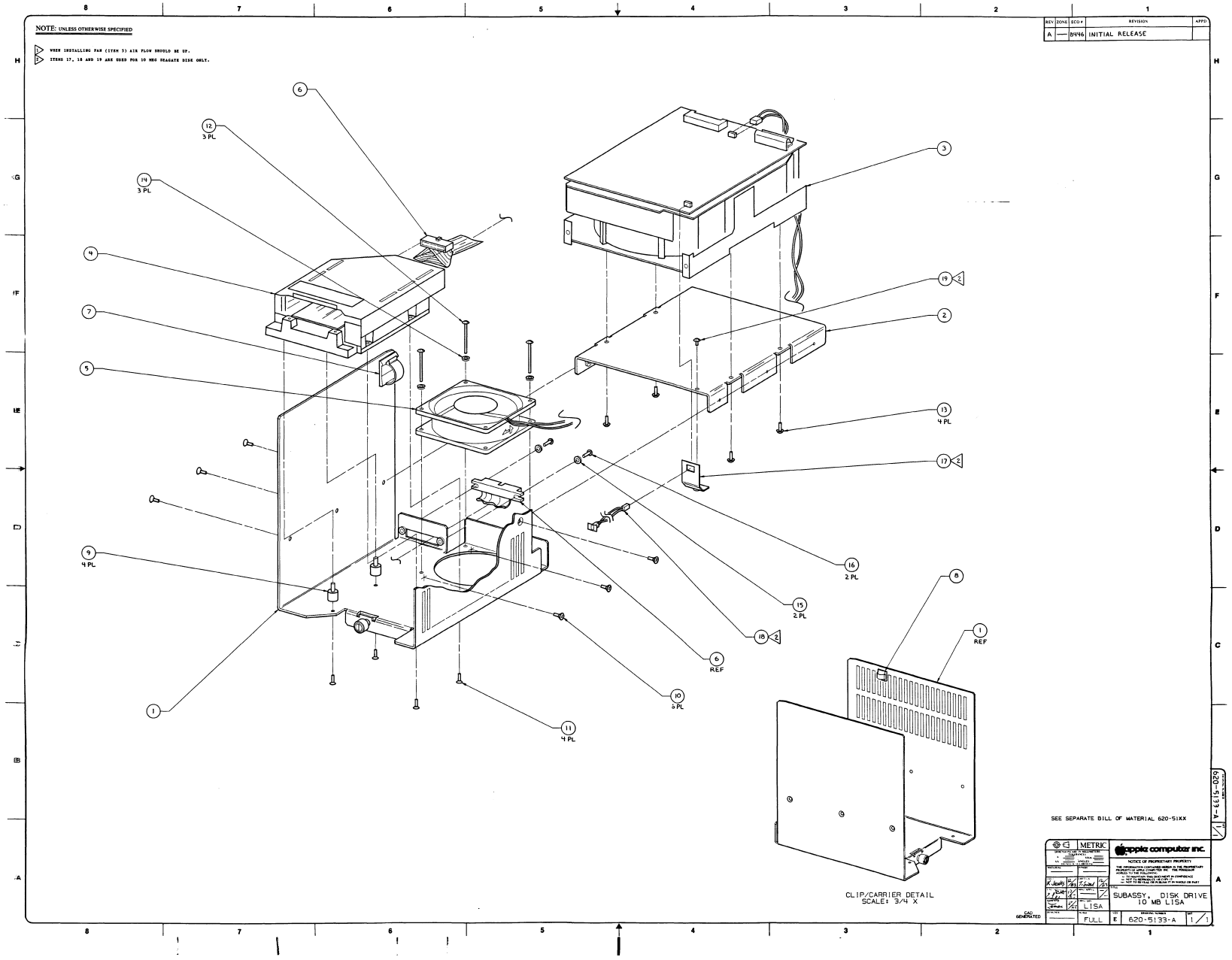
"APPLE_620-5129-A-2of2.PICT" 711 KB 2002-03-12 dpi: 200h x 200v pix: 8709h x 5646v



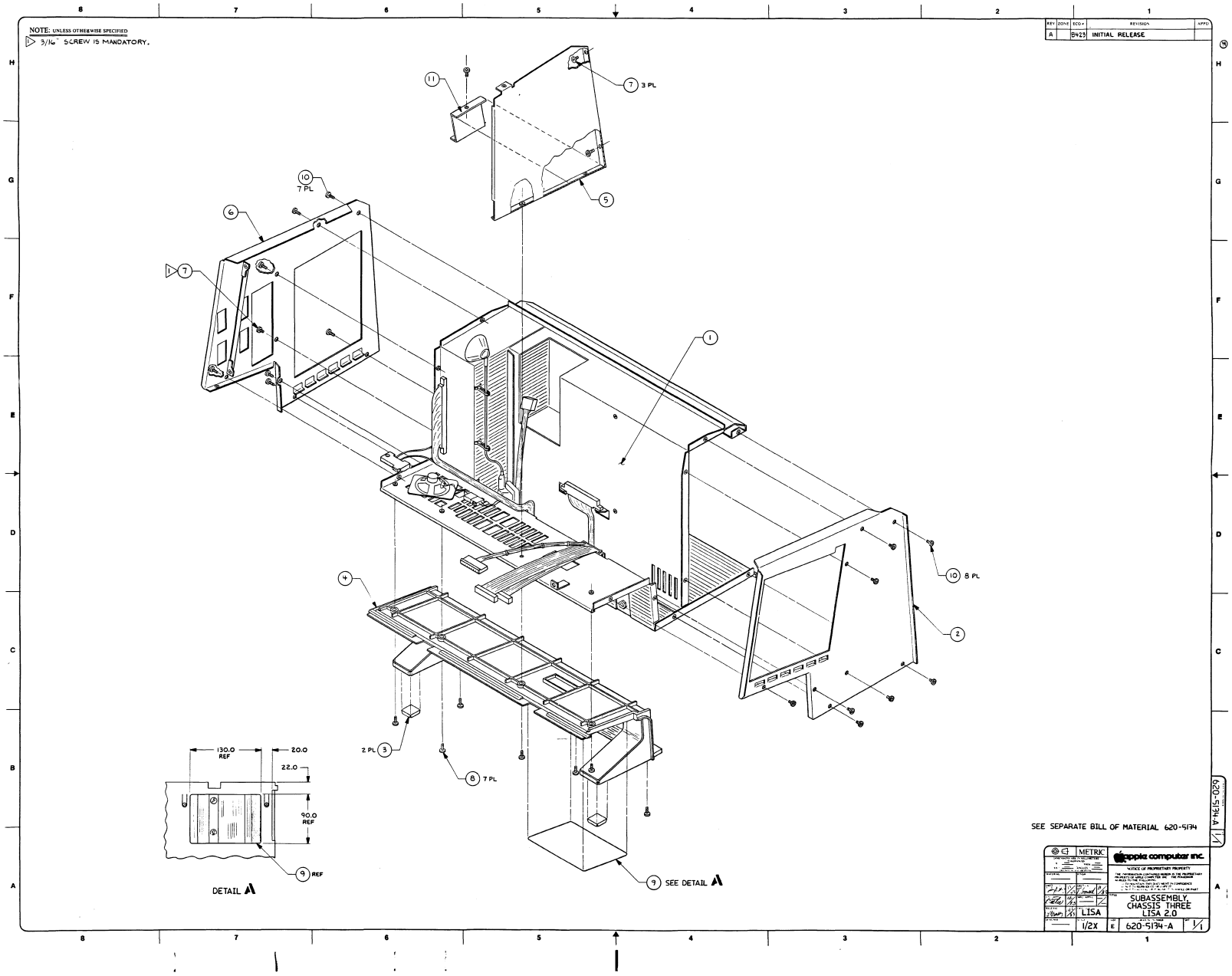
"APPLE_620-5130-A-1of1.PICT" 660 KB 2002-03-12 dpi: 200h x 200v pix: 8072h x 6172v



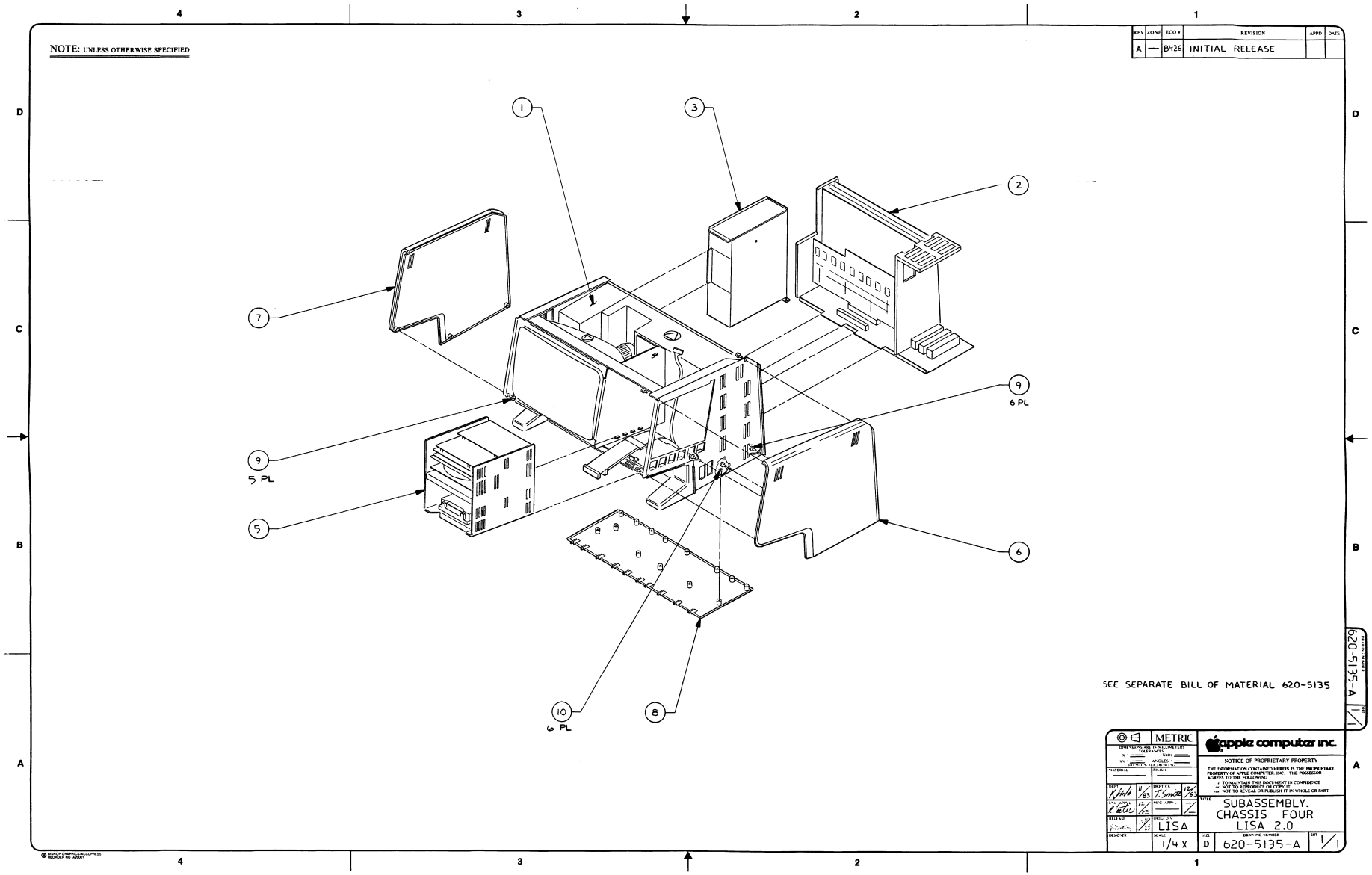
"APPLE_620-5132-A-1of1.PICT" 570 KB 2002-03-12 dpi: 200h x 200v pix: 8692h x 5699v



"APPLE_620-5133-A-1of1.PICT" 576 KB 2002-03-12 dpi: 200h x 200v pix: 7762h x 5993v



"APPLE_620-5134-A-1of1.PICT" 668 KB 2002-03-12 dpi: 200h x 200v pix: 7894h x 6078v

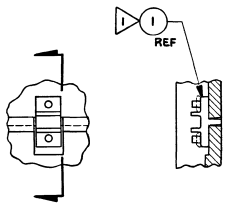


"APPLE_620-5135-A-1of1.PICT" 519 KB 2002-03-12 dpi: 200h x 200v pix: 8744h x 5681v

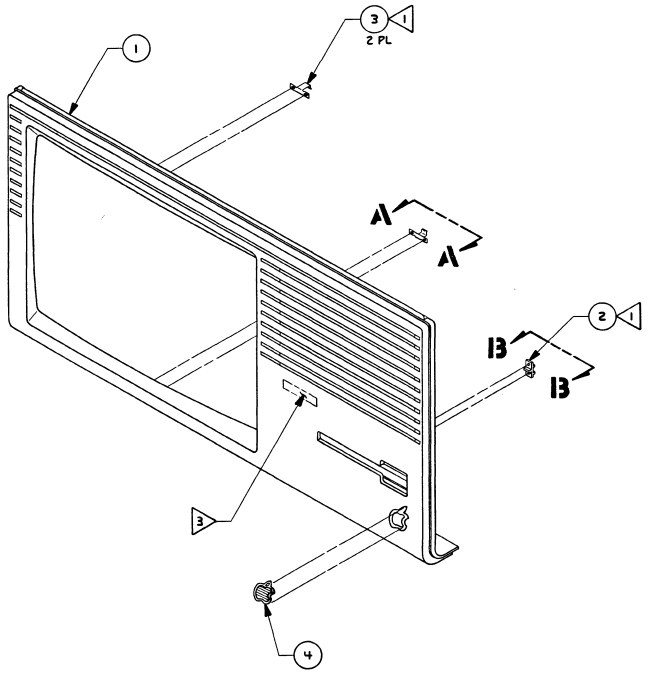
REV	ZONE	ECO #	REVISION	APPD	DATE
A		B439	INITIAL RELEASE		

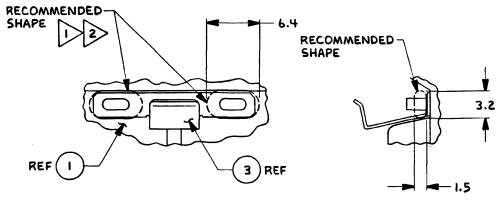
NOTE: UNLESS OTHERWISE SPECIFIED

1. HEAT STAKE/ULTRA SONIC WELD RETENTION CLIPS (ITEM 3) AND LED LENS (ITEM 2) TO BEZEL SECURELY SO THEY ARE TIGHT AGAINST INSIDE BEZEL SURFACE.
2. MATERIAL DISPLACEMENT AROUND PINS SHALL BE UNIFORM.
3. STAMP P/N AND REVISION ON BACKSIDE WITH 3.0 MM HIGH (MIN) LETTERS.



VIEW B-B
SCALE: 2X





VIEW A-A
SCALE: 4X
2 PL

SEE SEPARATE BILL OF MATERIAL 620-5136

DRAWING NUMBER 620-5136-A 1/1

METRIC

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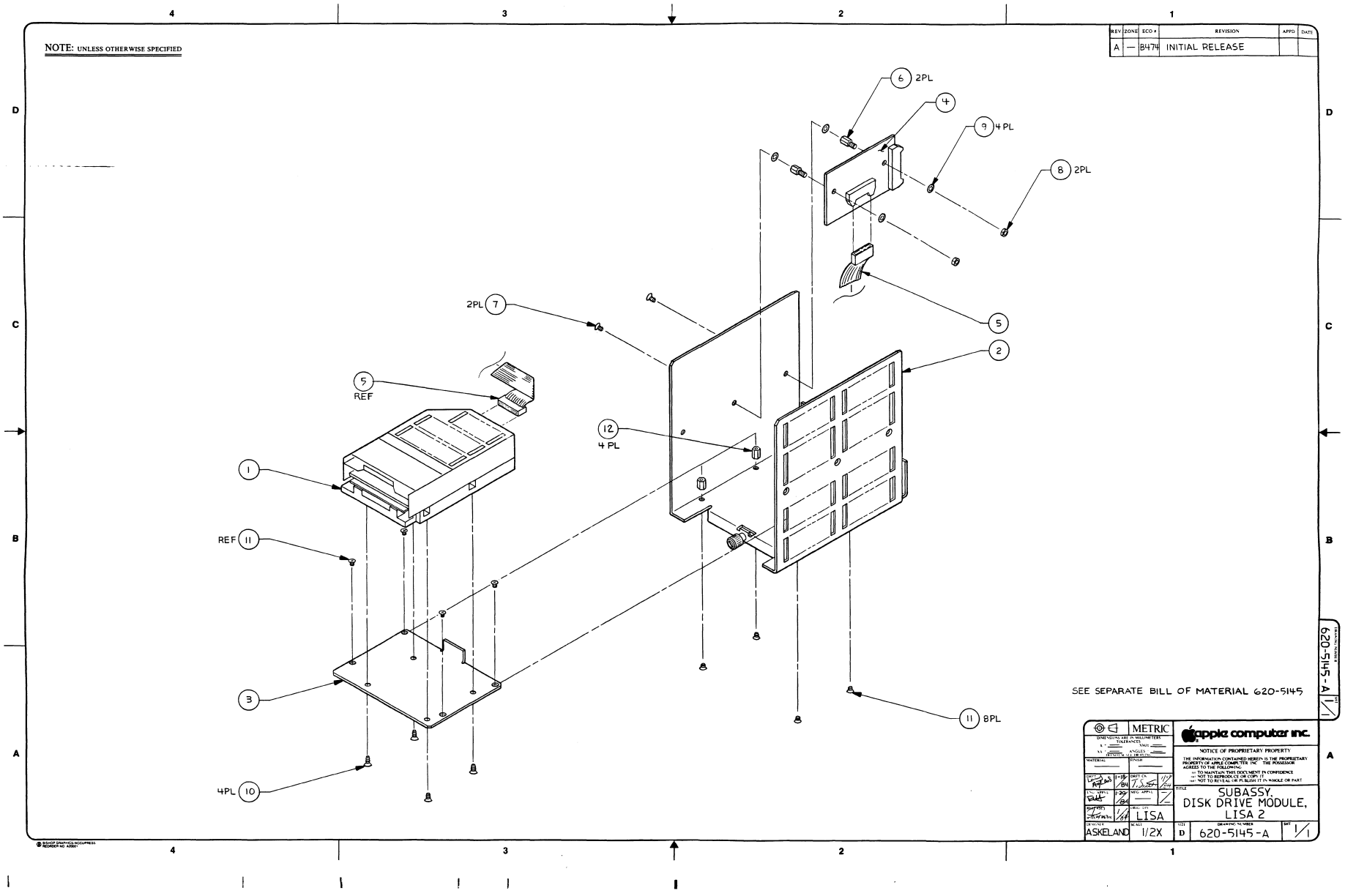
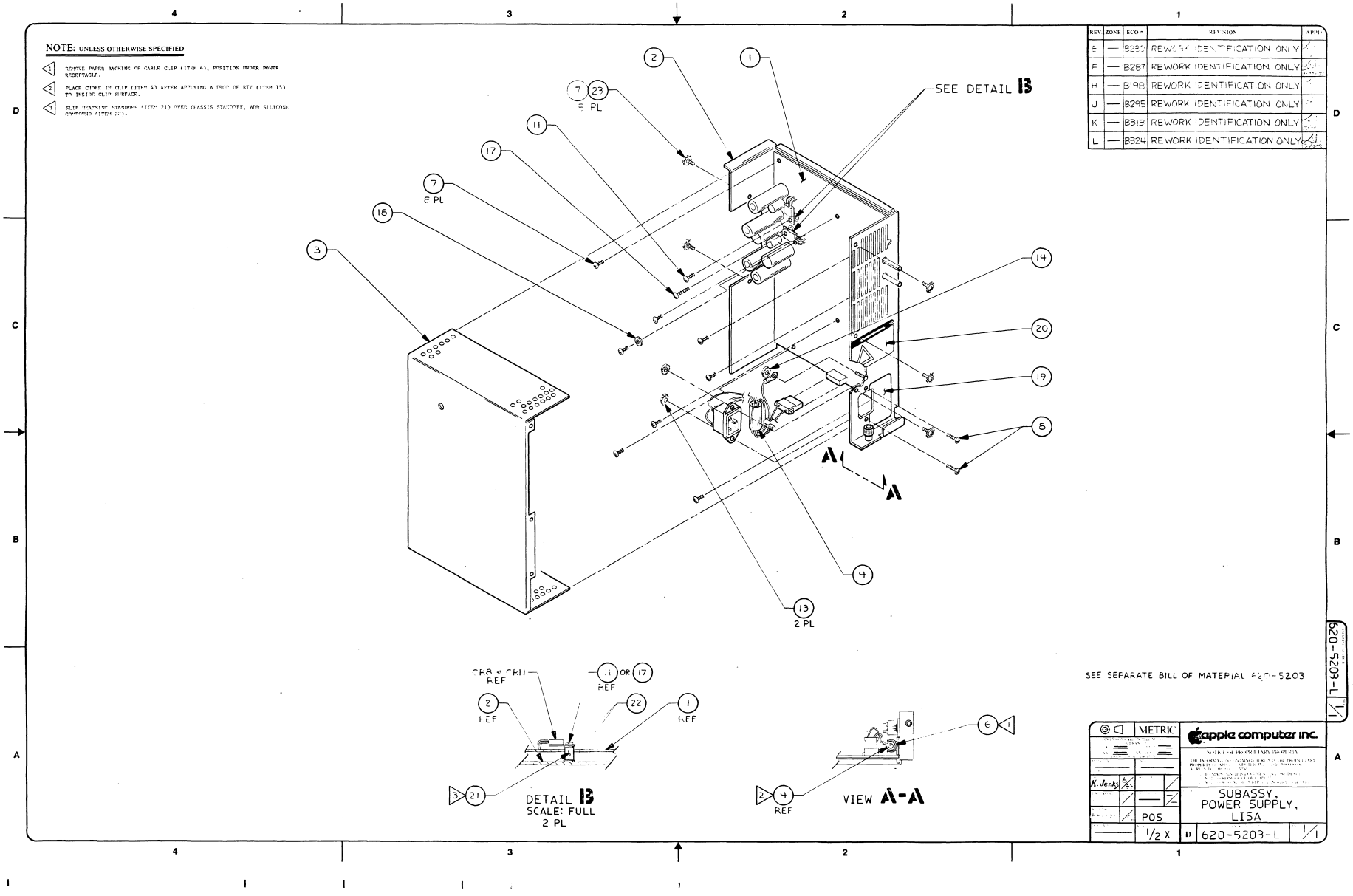
DRFT		DRFT CK	
ENG APPV		MFG APPV	
		CHKD BY	LISA
DESIGNER		SCALE	1/2X

TITLE: SUBASSY, BEZEL LISA.2.0

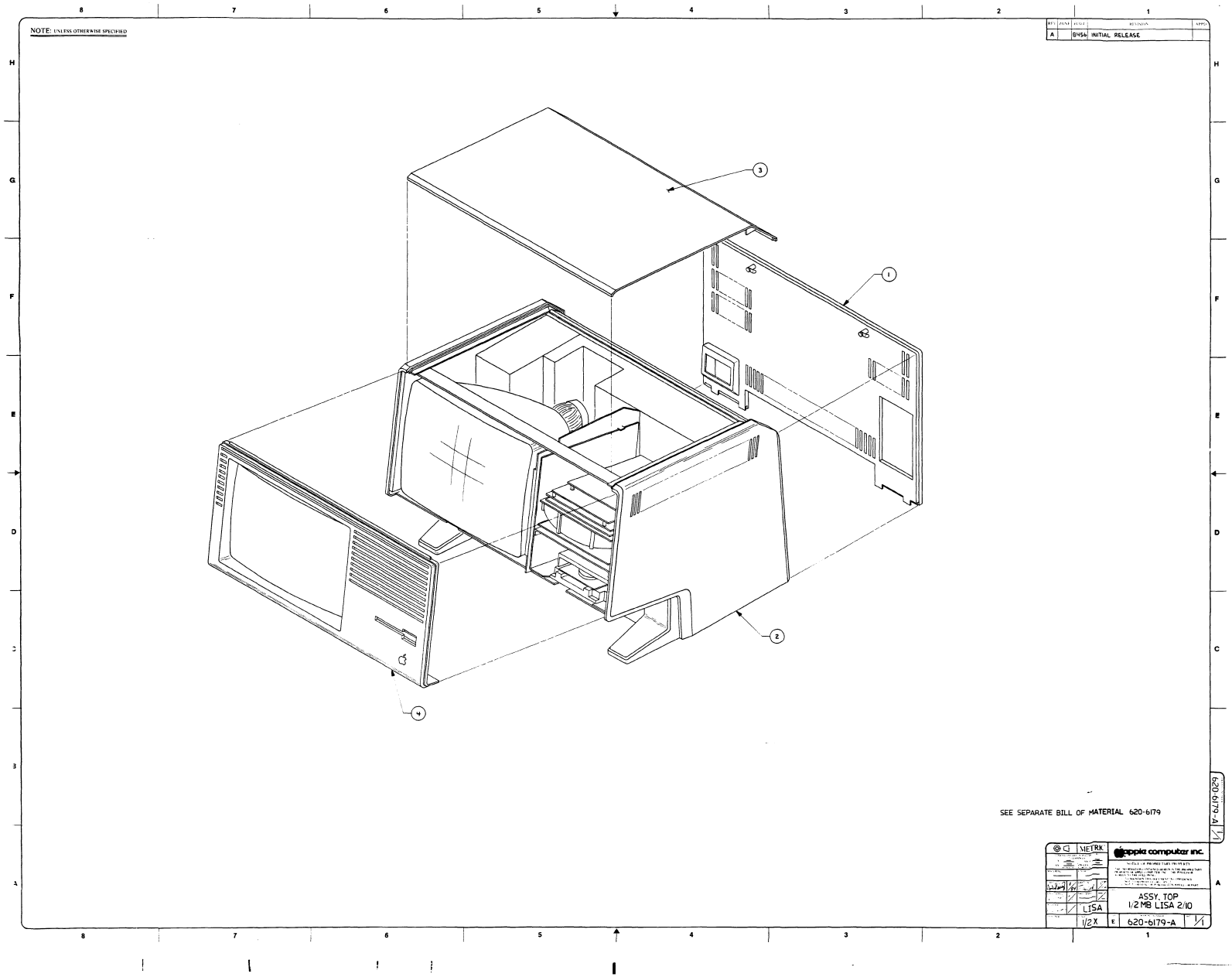
SIZE D | DRAWING NUMBER 620-5136-A | SHT 1/1



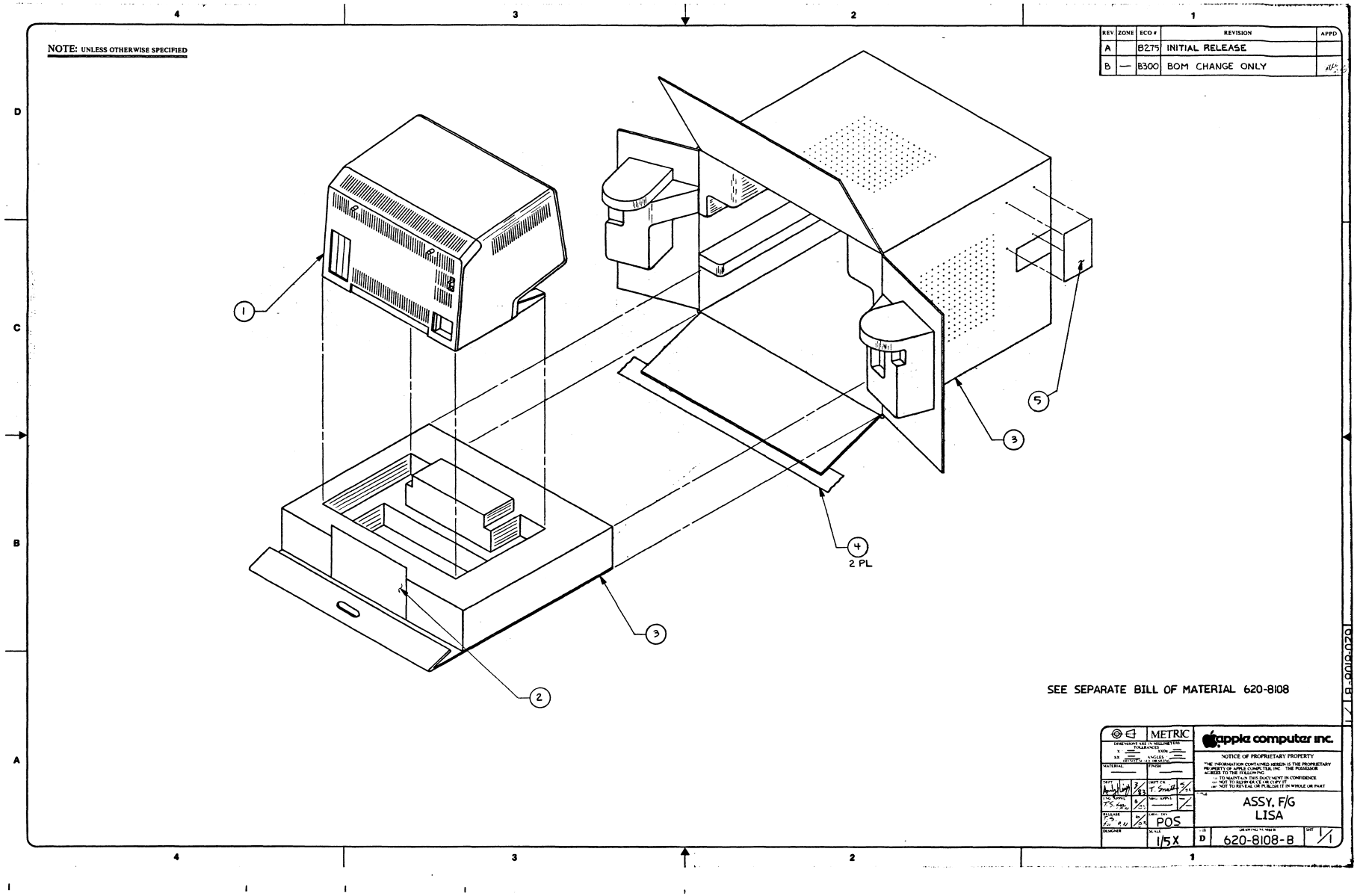
"APPLE_620-5145-A-1of1.PICT" 504 KB 2002-03-12 dpi: 200h x 200v pix: 8704h x 5794v



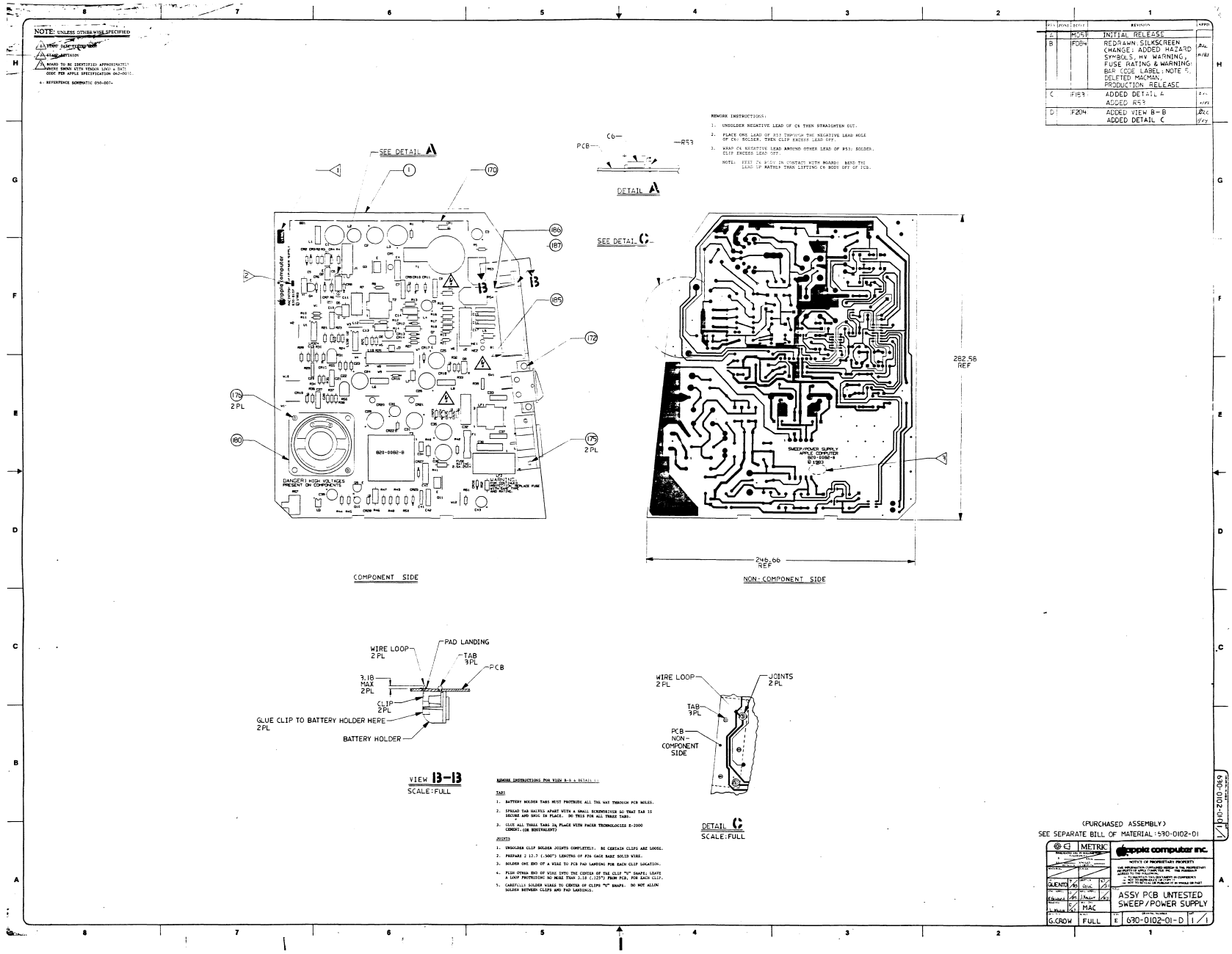
"APPLE_620-5203-L-1of1.PICT" 571 KB 2002-03-12 dpi: 200h x 200v pix: 8750h x 5749v



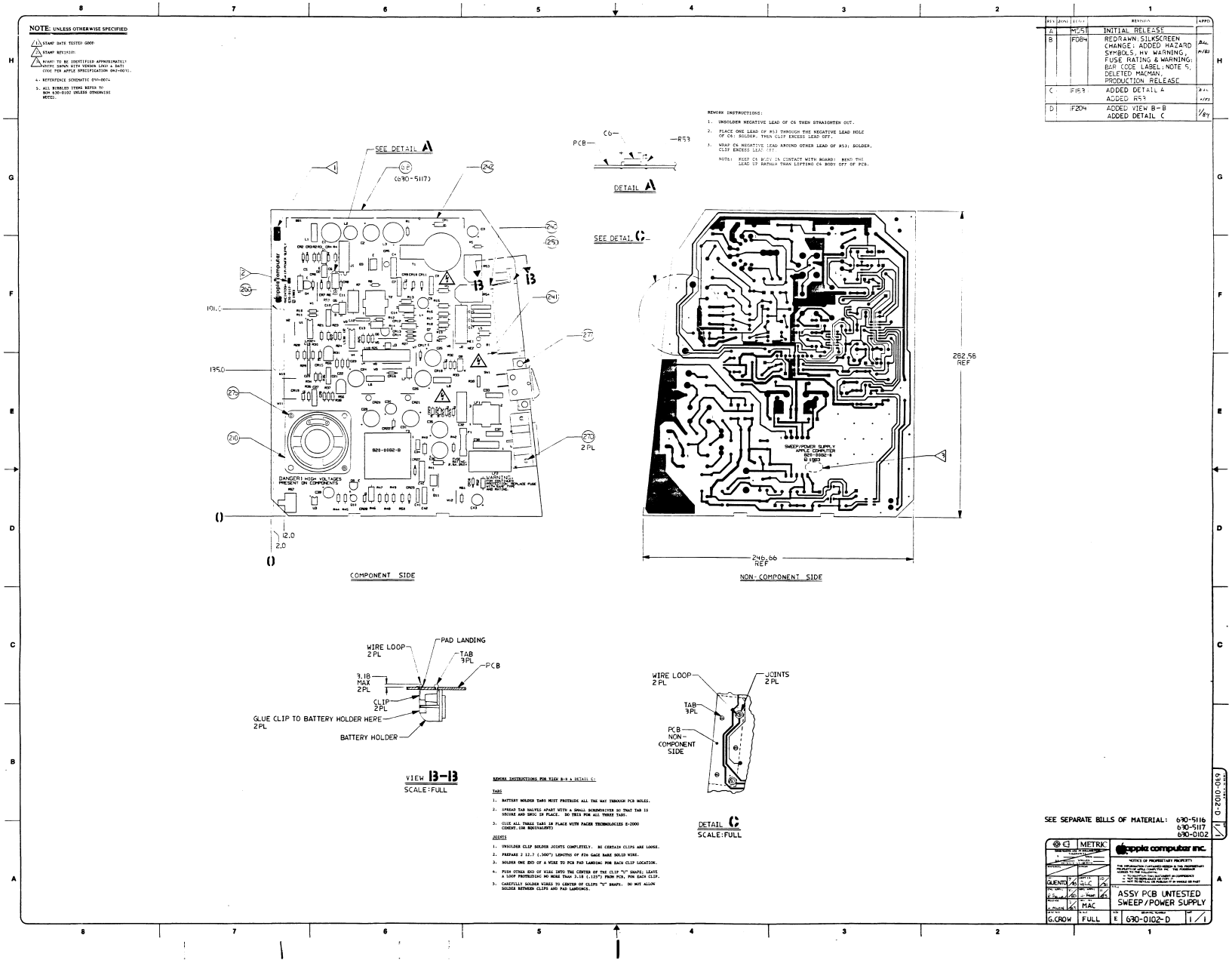
"APPLE_620-6179-A-1of1.PICT" 460 KB 2002-03-12 dpi: 200h x 200v pix: 7415h x 5772v



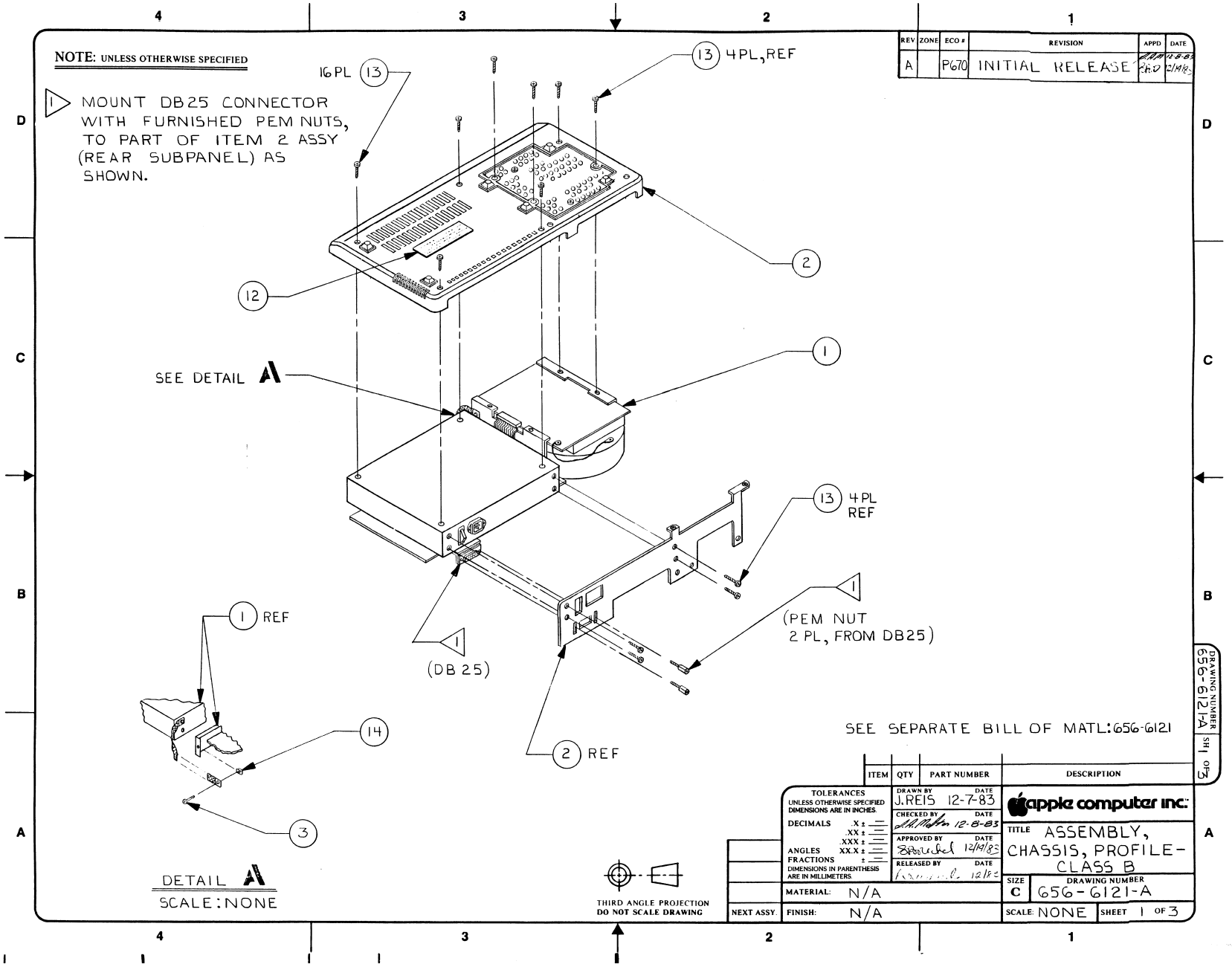
"APPLE_620-8108-B-1of1.PICT" 618 KB 2002-03-12 dpi: 200h x 200v pix: 8784h x 5702v



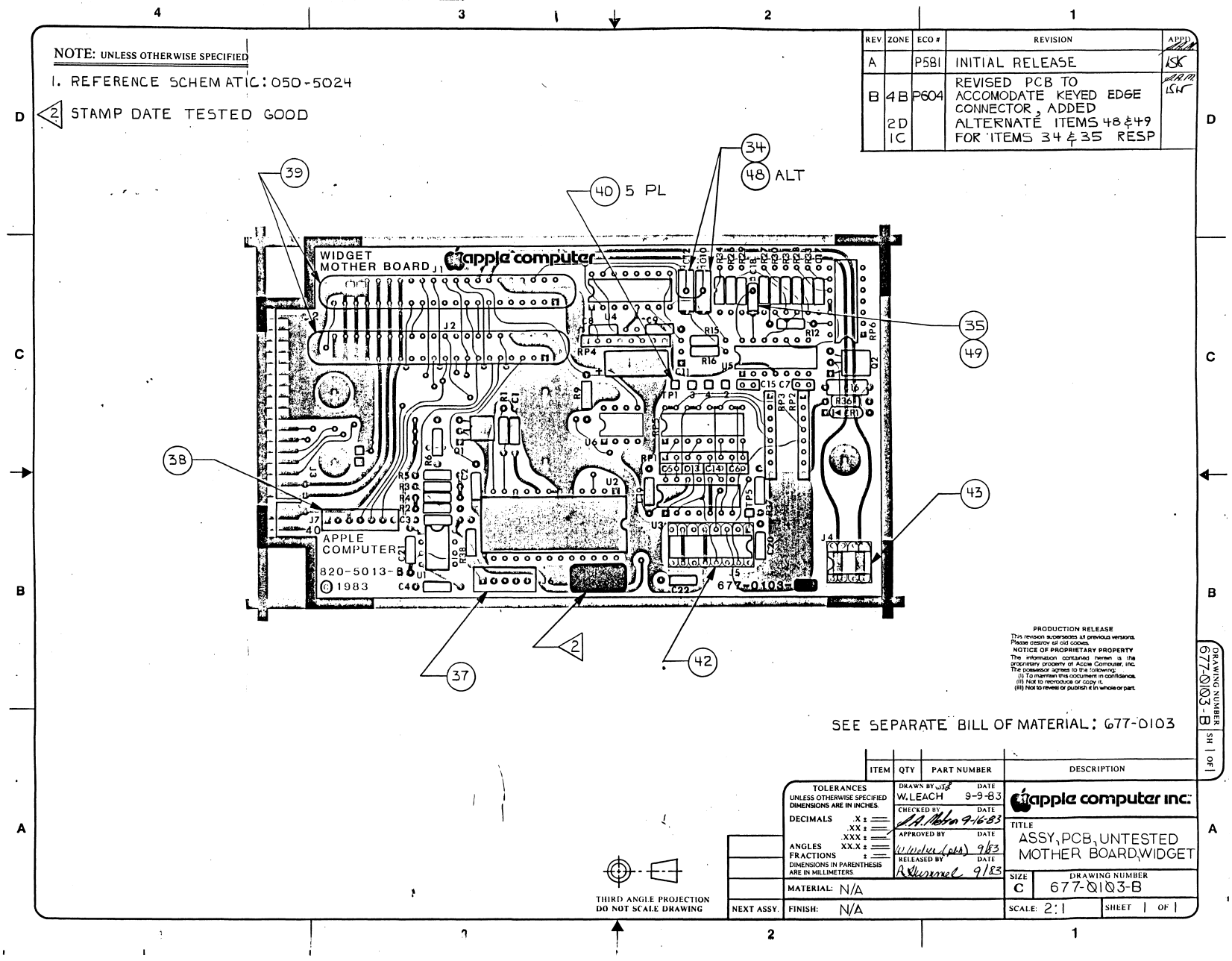
"APPLE_630-0102-01-D-1of1.PICT" 686 KB 2002-03-12 dpi: 200h x 200v pix: 7794h x 5945v



"APPLE_630-0102-D-1of1.PICT" 697 KB 2002-03-12 dpi: 200h x 200v pix: 8023h x 6106v



"APPLE_656-6121-A-1of3.PICT" 718 KB 2002-03-12 dpi: 200h x 200v pix: 8355h x 6452v

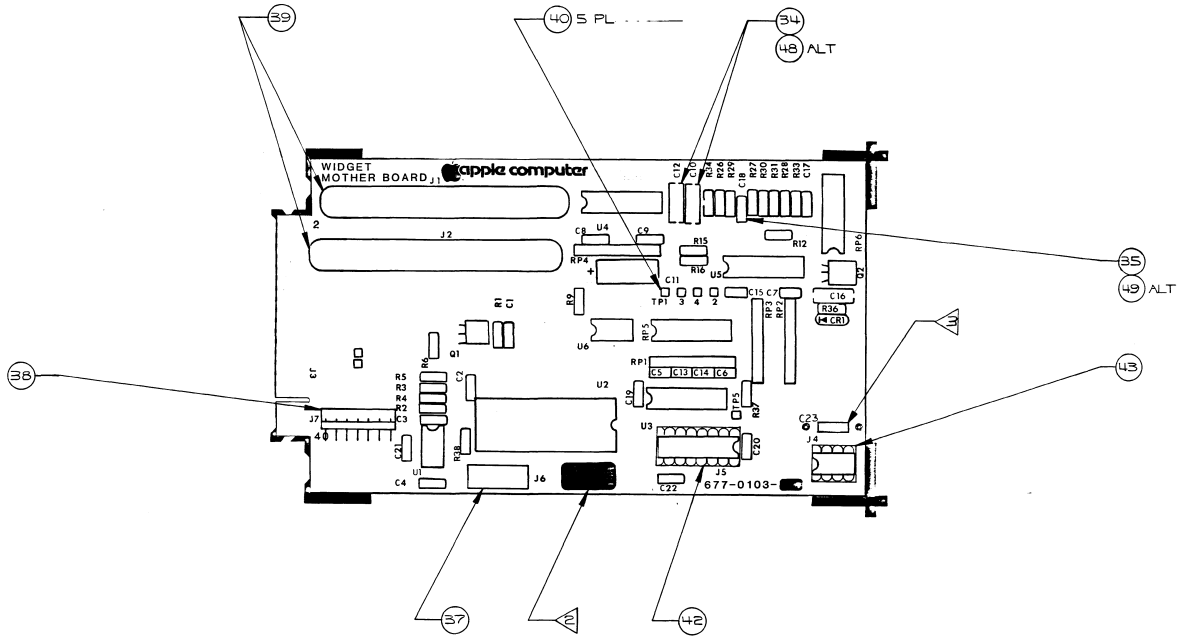


"APPLE_677-0103-B-1of1.PICT" 1229 KB 2002-03-12 dpi: 200h x 200v pix: 8356h x 6475v

NOTE: UNLESS OTHERWISE SPECIFIED

1. REFERENCE SCHEMATIC : 050-5024 .
2. STAMP DATE TESTED GOOD .
3. "NO CAPACITOR REQUIRED FOR C23 LEAVE EMPTY (DO NOT LOAD)."

REV	ZONE	ECO #	REVISION	APPD	DATE
C	2B	P633	REVISED & REDRAWN WITH CHANGE, ADDED ITEM 50, ADDED NOTE 3	MK	12/15/83



SEE SEPARATE BILL OF MATERIAL : 677-0103

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS X ± XX ± XXX ± XX.X ±
ANGLES ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS

DRAWN BY W. EACH 9-83 DATE
CHECKED BY DATE
APPROVED BY W. WEBER 12/83 DATE
RELEASED BY DATE

apple computer inc.

TITLE ASSY, PCB, UNTESTED MOTHER BOARD, WIDGET

MATERIAL
FINISH
NEXT ASSY

SIZE D | DRAWING NUMBER 677-0103-C
SCALE 2:1 | SHEET 1 OF 1

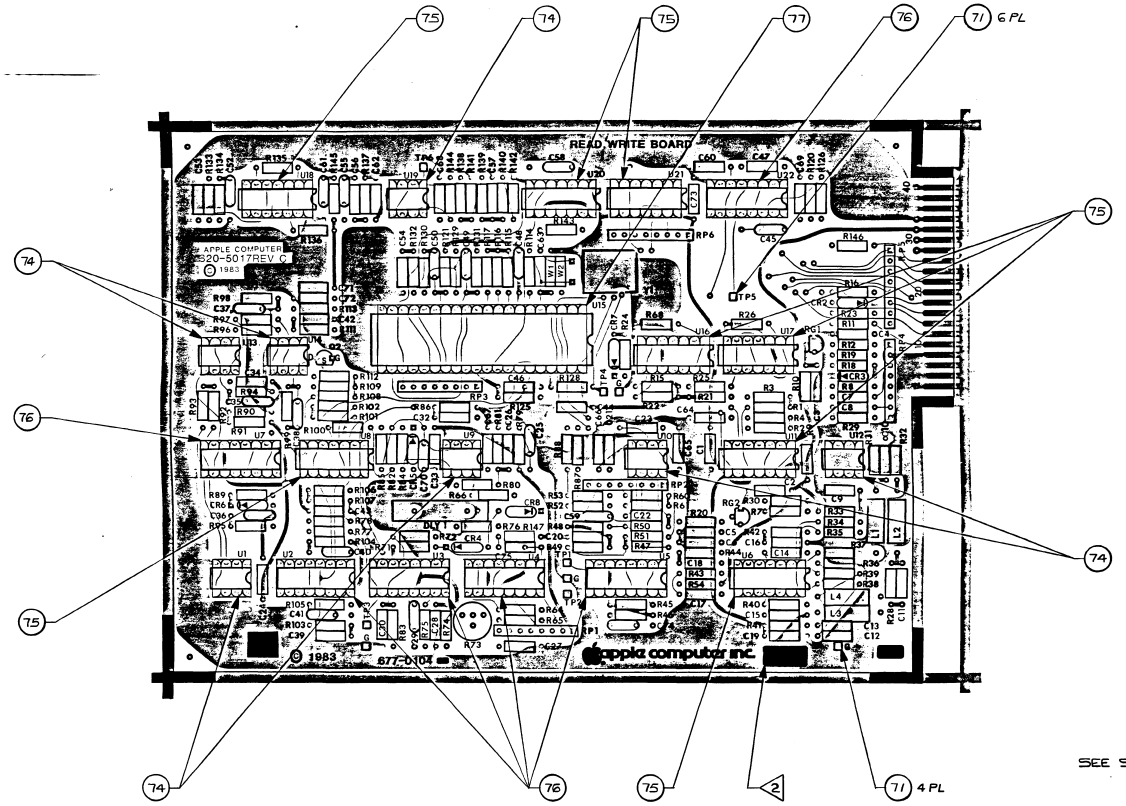
THIRD ANGLE PROJECTION DO NOT SCALE DRAWING

"APPLE_677-0103-C-1of1.PICT" 463 KB 2002-03-12 dpi: 200h x 200v pix: 8688h x 5567v

NOTE: UNLESS OTHERWISE SPECIFIED

1. REFERENCE SCHEMATIC: 050-5028
2. STAMP DATE TESTED GOOD.

REV	ZONE	ECO #	REVISION	APPD	DATE
C		P661	REVISED AND REDRAWN WITH CHANGE		



SEE SEPARATE BILL OF MATERIALS: 677-0104

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS X ± XX ± XXX ±
ANGLES ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS
MATERIAL:
NEXT ASSY
FINISH:

DRAWN J. MELTON 11/83
CHECKED BY
APPROVED BY B. WONG 12/83
RELEASED BY

appleⅡ computer inc.

TITLE ASSY, PCB, UNTESTED READ/WRITE BOARD WIDGET
SIZE D
DRAWING NUMBER 677-0104-C
SCALE NONE
SHEET 1 OF 1

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWING NUMBER 677-0104-C SHT 1 OF 1

"APPLE_677-0104-C-1of1.PICT" 1048 KB 2002-03-12 dpi: 200h x 200v pix: 8825h x 5657v

REV.	ZONE	ECO #	REVISION	APPD
A		P565	INITIAL RELEASE (SK-W159-03)	
A	4C 4B	P630	REVISED NOTE 5: FORWARD BIASING ≤2V WAS ≥2V & REVERSE BIASING ≤0.5μA WAS ≥0.5μA	

NOTE: UNLESS OTHERWISE SPECIFIED

1. SEE SHEET-2 FOR INSTALLATION OF FLEXCABLE (ITEM 6) AND ASSOCIATED HARDWARE.
2. BEND FLEXCABLE (ITEM 6) AS SHOWN. PRIOR TO ASSEMBLY, REMOVE ALL COVERING TO EXPOSE ADHESIVE EXCEPT WHERE NOTED - SEE NOTE 3.
3. COVERING OVER ADHESIVE TO REMAIN INTACT IN INDICATED AREAS.
4. MOUNTING HOLES TO BE CONCENTRIC AFTER BENDING.
5. ELECTRICAL SPECIFICATION

CONNECTOR:

PIN 1 LED-
2 SENSOR CHIP; SEGMENT B̄
3 SENSOR CHIP; GROUND
4 SENSOR CHIP; SENSOR B
5 GROUND SHIELDS; COMMON WITH 12
6 HEAD 1
7 HEAD 1; CENTER
8 HEAD 1
9 HEAD 2
10 HEAD 2; CENTER
11 HEAD 2
12 GROUND SHIELDS; COMMON WITH 5
13 SENSOR CHIP; SEGMENT A
14 SENSOR CHIP; FEED-BACK SEGMENT FOR AGC
15 SENSOR CHIP; SENSOR CHIP; SEGMENT Ā
16 LED +

MINIMUM OUTPUT (THROUGH RETICLE)

INPUT PIN - PIN			OUTPUT PIN - PIN	
1 (-)	16 (+)	25 mA	3 - 2	≥ 7 μA
1	16		3 - 4	≥ 7
1	16		~~3 - 13~~	≥ 7
1	16		3 - 14	≥ 20μA
1	16		3 - 15	≥ 7

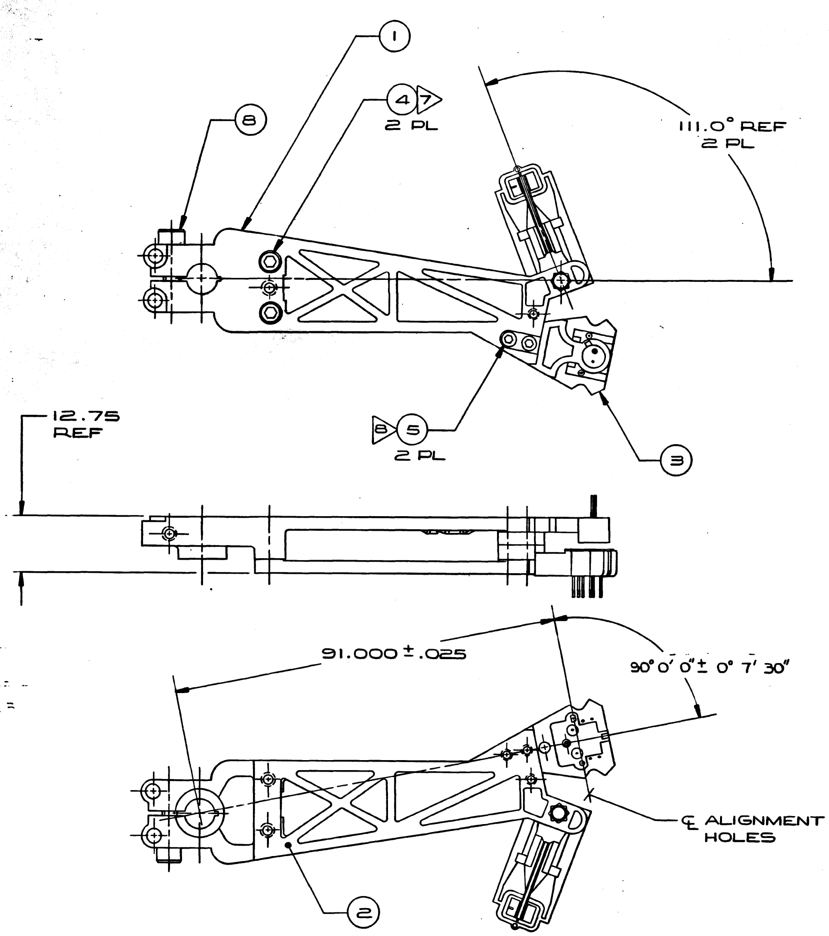
FORWARD BIASING (INTERNAL IMPEDENCE)

3 (+)	2 (-)	10mA	≤ 2V
3	4		
3	13		
3	14		
3	15		

REVERSE BIASING (DARK CURRENT)

3 (-)	2 (+)	0.5V	≤ 0.5μA
3	4		
3	13		
3	14		
3	15		

6. TRIM LEADS TO DIMIENSIONS SHOWN AFTER SOLDERING.
7. TORQUE SCREWS (ITEM 4) TO 5.5 IN/LBS.
8. TORQUE SCREWS (ITEM 5) TO 3.0 IN/LBS.



1 FLEXCABLE (ITEM 6) OMITTED FOR CLARITY

SEE SEPARATE BILL OF MATERIAL : 677-5013

METRIC

DIMENSIONS ARE IN MILLIMETERS

DRFT: ANDERSON 6/83 | DRFT CK: A.A.M. 10/83 | ENG APPVL: 10/83 | MFG APPVL | RELEASE: 1/83 | ORIG. DIV: M.S.D. | SCALE: 2X

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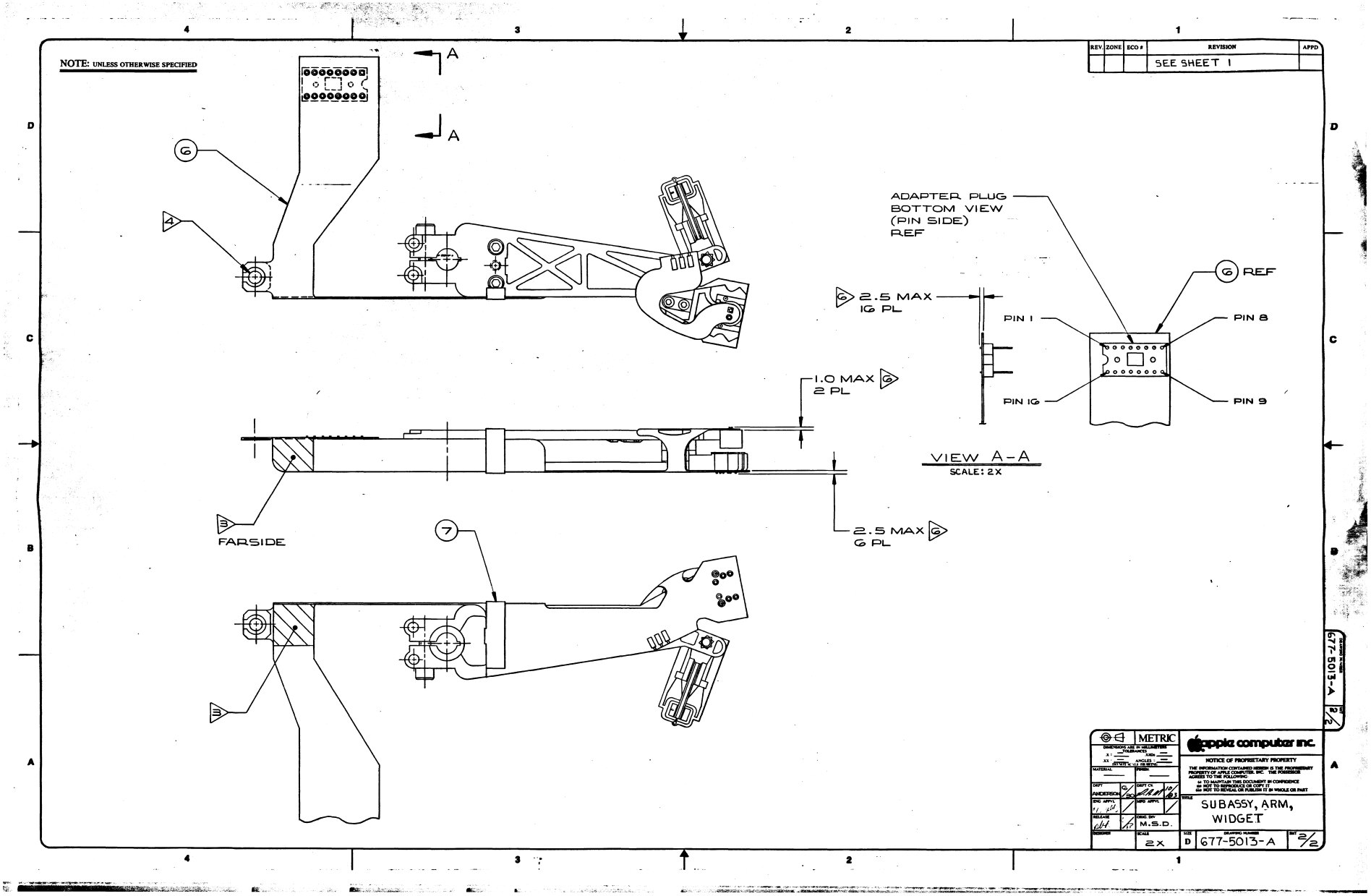
TITLE: SUBASSY, ARM, WIDGET

SIZE: D | DRAWING NUMBER: 677-5013-A | SHT 1/2

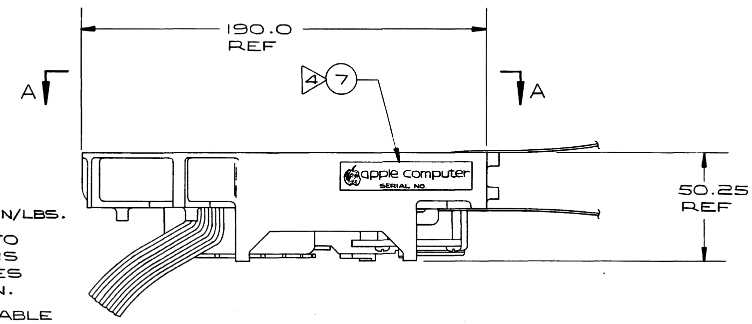
“APPLE_677-5013-A-1of2.PICT” 786 KB 2002-03-12 dpi: 200h x 200v pix: 8626h x 5636v

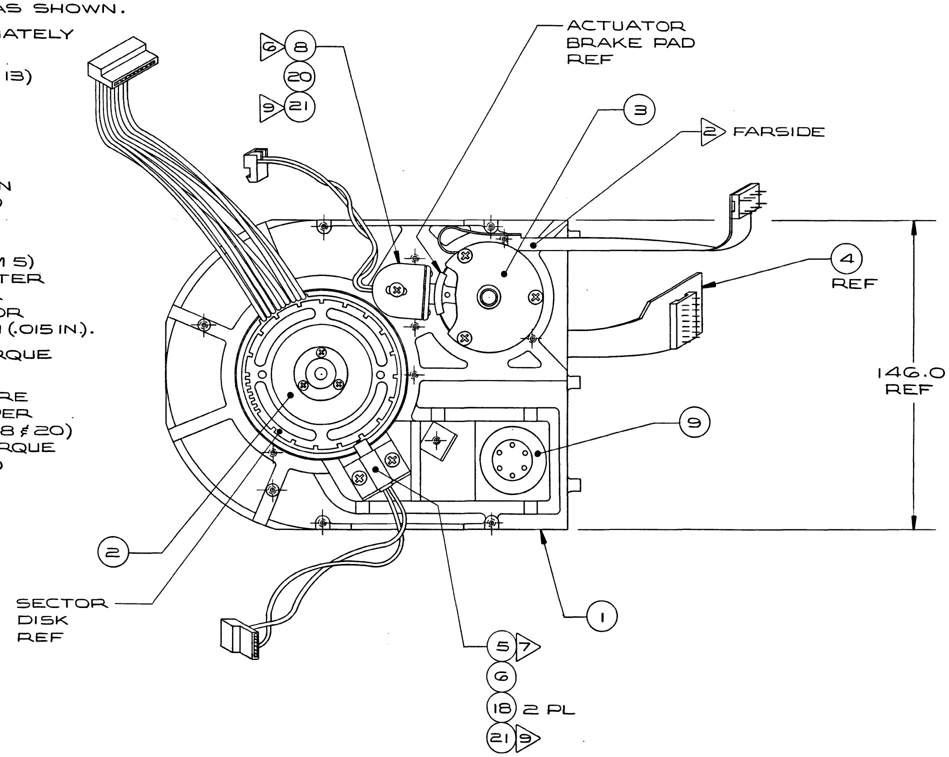


"APPLE_677-5013-A-2of2.PICT" 570 KB 2002-03-12 dpi: 200h x 200v pix: 8678h x 5698v

NOTE: UNLESS OTHERWISE SPECIFIED

1. ALIGN ARM ASSY (ITEM 4) TO ACTUATOR MOTOR ASSY (ITEM 3) BY FOLLOWING THE PROCEDURES LISTED BELOW:
   A. ROTATE ARM ASSY CLOCKWISE (LOOKING AT VIEW A-A) UNTIL LOWER ARM CONTACTS 7.0 DIA BOSS ON CHASSIS.
   B. ROTATE ACTUATOR SHAFT CLOCKWISE (LOOKING AT VIEW A-A) AS FAR AS POSSIBLE.
   C. TIGHTEN 6-32 SCREW ON ARM TO 15.0±1.0 IN/LBS.
2. PRIOR TO ASSEMBLY, REMOVE COVERING TO EXPOSE ADHESIVE ON FLEXCABLES (SEE ITEMS 3 AND 4) IN LOCATIONS SHOWN. FLEXCABLES TO BE ROUTED APPROXIMATELY AS SHOWN.
3. AFTER ASSEMBLY, 3.81 DIA HOLE IN FLEXCABLE (SEE ITEM 4) TO BE CONCENTRIC WITH 6-32 TAPPED HOLE IN CHASSIS (ITEM 1) AS SHOWN.
4. POSITION LABEL (ITEM 7) APPROXIMATELY AS SHOWN.
5. PRESS FIT ALIGNMENT PINS (ITEM 13) INTO 1.580 DIA HOLES IN CHASSIS (ITEM 1) TO INDICATED DIMENSION.
6. POSITION BRAKE ASSY (ITEM 8) SO THAT BRAKE HOUSING CENTER LINE IS RADIAL TO ACTUATOR SHAFT. AIR GAP BETWEEN NEOPRENE PAD ON BRAKE AND ACTUATOR BRAKE PAD TO BE .330 (.013 IN.) WHEN BRAKE IS ENERGIZED.
7. POSITION INDEX SENSOR ASSY (ITEM 5) SO THAT SENSOR HOUSING CENTER LINE IS RADIAL TO SPINDLE MOTOR SHAFT. AIR GAP BETWEEN SENSOR TIP AND SECTOR DISK TO BE .381 (.015 IN.).
8. UNLESS OTHERWISE SPECIFIED, TORQUE ALL SCREWS TO 10.0 IN/LBS.
9. AFTER BRAKE AND INDEX SENSOR ARE PROPERLY POSITIONED ON CHASSIS PER NOTES 6 & 7 AND SCREWS (ITEMS 18 & 20) ARE TORQUED IN PLACE, APPLY TORQUE SEAL (ITEM 21) TO SCREW HEADS TO PREVENT TAMPERING.





REV.	ZONE	ECO #	REVISION	APPD
A		P619	INITIAL RELEASE (SK-W174-05)	

SEE SEPARATE BILL OF MATL: 677-5016

METRIC — DIMENSIONS ARE IN MILLIMETERS

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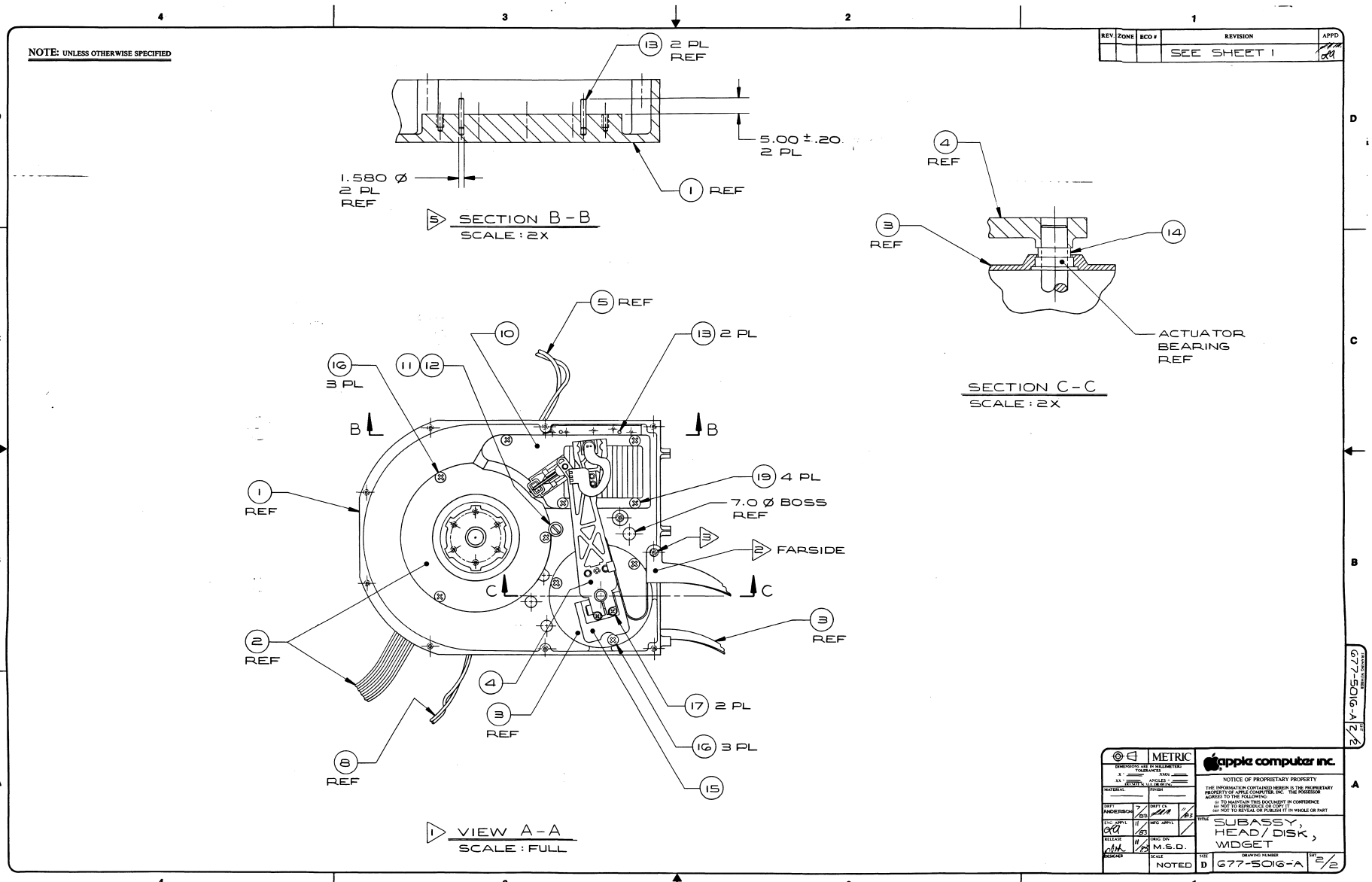
DRFT: ANDERSON 7/83
ORIG DIV: M.S.D.
SCALE: FULL

TITLE: SUBASSY, HEAD / DISK WIDGET

SIZE: D DRAWING NUMBER: 677-5016-A SHT 1/2

“APPLE_677-5016-A-1of2.PICT” 877 KB 2002-03-12 dpi: 200h x 200v pix: 8672h x 5713v

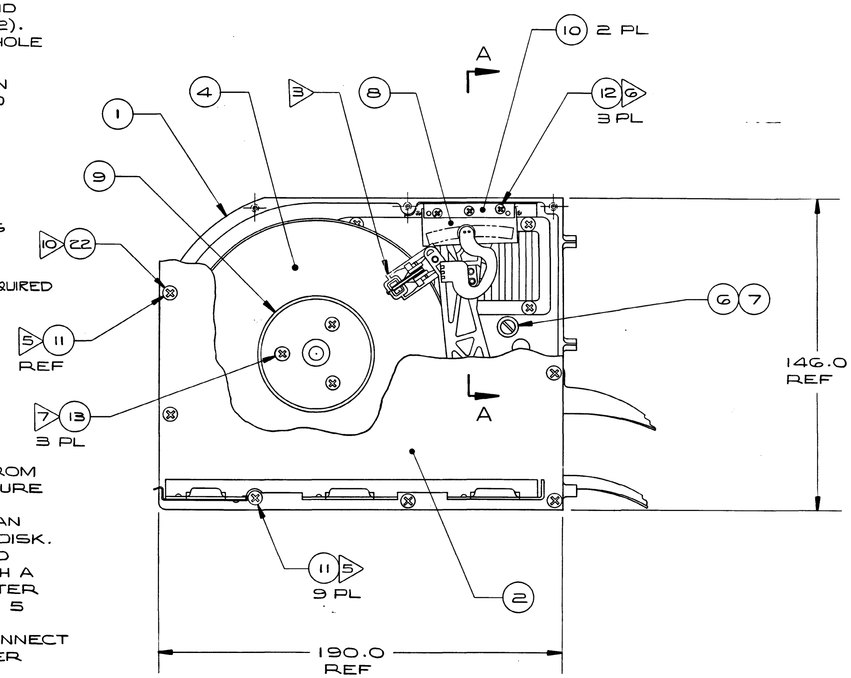


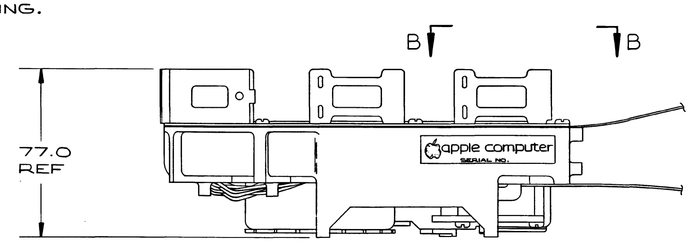
"APPLE_677-5016-A-2of2.PICT" 555 KB 2002-03-12 dpi: 200h x 200v pix: 8657h x 5611v

REV.	ZONE	ECO #	REVISION	APPD
A		PG20	INITIAL RELEASE (SK-W175-04)	

NOTE: UNLESS OTHERWISE SPECIFIED

1. PRIOR TO ASSEMBLY, REMOVE COVERING FROM GASKET (ITEM 3) TO EXPOSE ADHESIVE AND PRESS ONTO UNDERSIDE OF COVER (ITEM 2). CARE MUST BE TAKEN TO ENSURE THAT HOLE PATTERNS LINE UP.
2. INSTALL PLUG (ITEM 5) IN COVER (ITEM 2) IN LOCATION SHOWN. PLUG MUST NOT EXTEND BEYOND TOP SURFACE OF COVER.
3. TO LOAD HEADS ONTO DISK (ITEM 4) SLIDE HEAD LOADING TOOL BETWEEN UPPER AND LOWER ARMS TO GENTLY FORCE HEADS APART. ROTATE ARM ASSY UNTIL HEADS ARE OVER DISK AND CAREFULLY REMOVE HEAD LOADING TOOL. HEADS ARE NOW PROPERLY POSITIONED ON DISK.
4. INSTALL SHIMS (ITEMS 15 THRU 21) AS REQUIRED IN LOCATION SHOWN TO ACHIEVE THE INDICATED GAP BETWEEN BOTTOM SURFACE OF SCALE (ITEM 8) AND TOP SURFACE OF RETICLE.
5. TORQUE SCREWS (ITEM 11) TO 10.0 IN/LBS.
6. TORQUE SCREWS (ITEM 12) TO 3.0 IN/LBS.
7. TORQUE SCREWS (ITEM 13) TO 5.0 IN/LBS.
8. PARTICLE COUNT PROCEDURE: AFTER ASSY, REMOVE PLUG (ITEM 5) FROM COVER AND INSERT AIR SAMPLING FIXTURE FROM PARTICLE COUNTER INTO HOLE. CONNECT SPINDLE MOTOR HARNESS TO AN EXTERNAL POWER SUPPLY TO ROTATE DISK. PARTICLE COUNT READING SHOULD BE 50 PARTICLES PER CUBIC FT OR LESS WITH A MAX PARTICLE SIZE OF .3 MICRONS AFTER RUNNING THE UNIT FOR NO MORE THAN 5 MINUTES. AFTER TEST IS COMPLETED, INSTALL PLUG PER NOTE 2 AND DISCONNECT SPINDLE MOTOR HARNESS FROM POWER SUPPLY. DO NOT MOVE CHASSIS UNTIL SPINDLE MOTOR HAS STOPPED ROTATING.
9. AFTER PARTICLE COUNT TESTING PER NOTE 8, POSITION LABEL (ITEM 14) OVER PLUG APPROXIMATELY AS SHOWN.
10. AFTER COVER IS IN PLACE AND ALL SCREWS (ITEM 11) ARE PROPERLY TORQUED PER NOTE 5, APPLY TORQUE SEAL (ITEM 22) TO SCREW HEAD TO PREVENT TAMPERING (ONE PLACE ONLY IN LOCATION SHOWN).

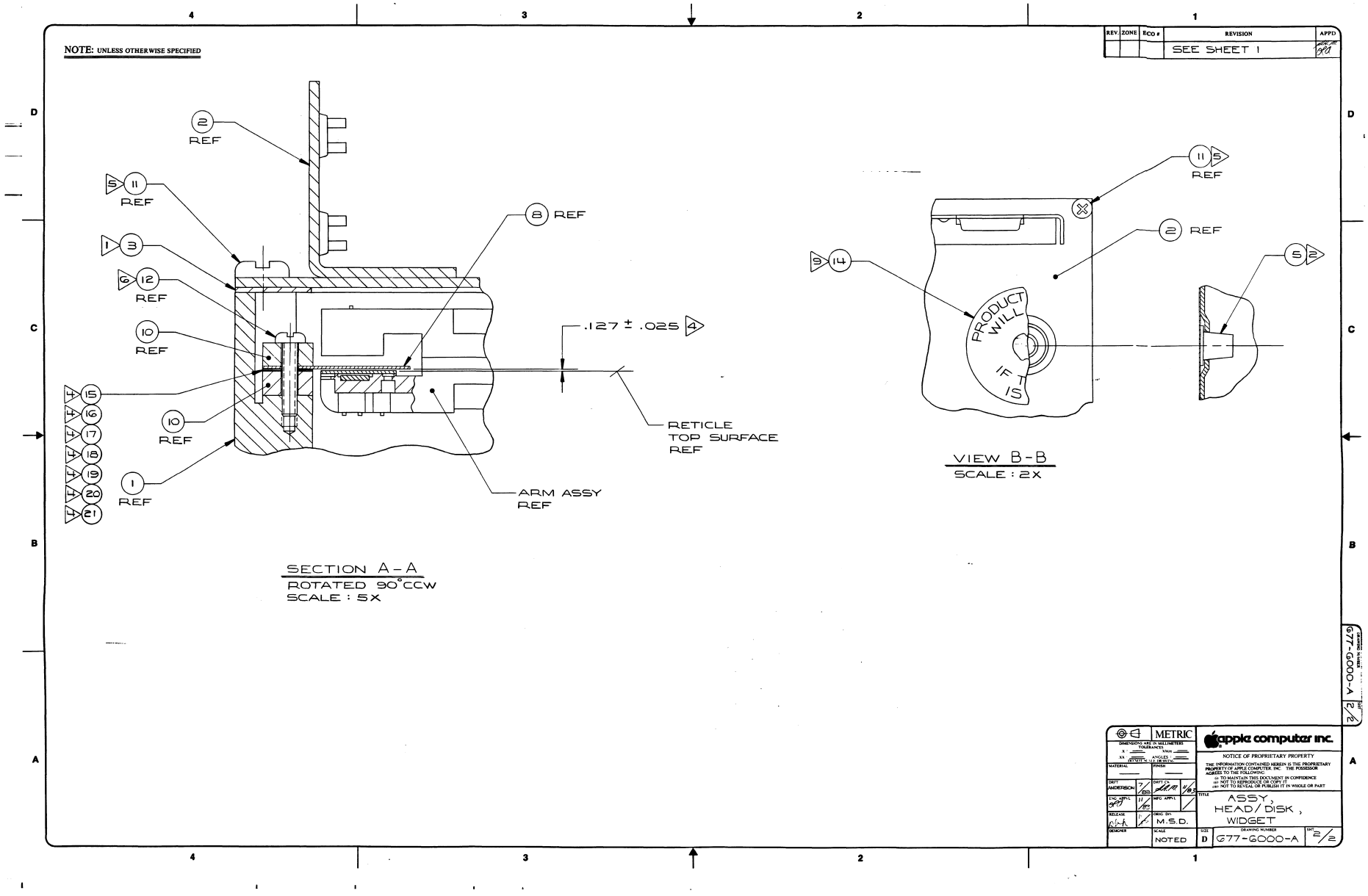




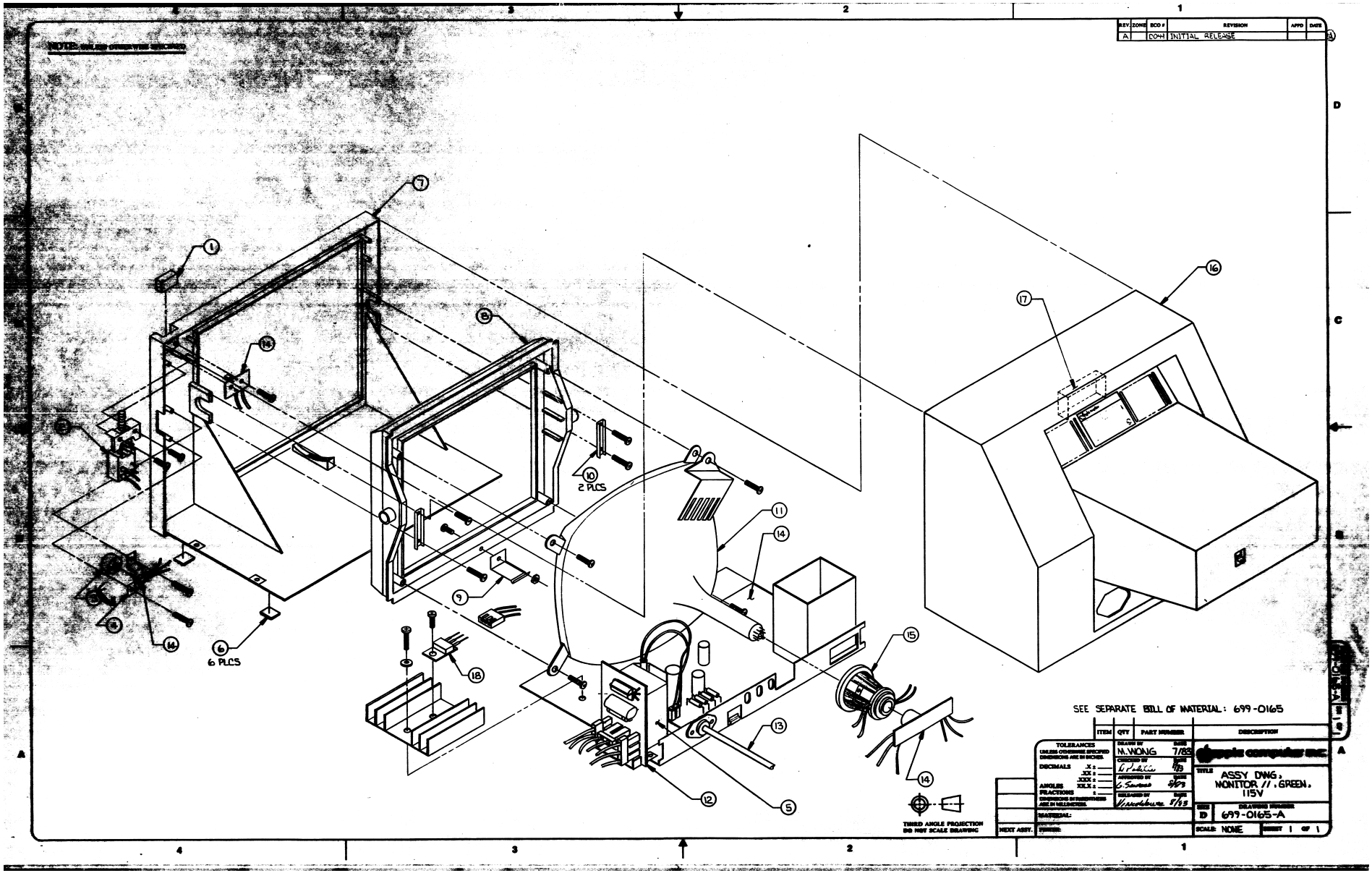
SEE SEPARATE BILL OF MAT'L 677-6000

METRIC	apple computer inc.
DIMENSIONS ARE IN MILLIMETERS TOLERANCES .X ± .XX ± .XXX ± ANGLES ± DO NOT SCALE DRAWING	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING (i) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE (ii) NOT TO REPRODUCE OR COPY IT (iii) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
MATERIAL — FINISH —	
DRFT ANDERSON 7/83; DRFT CK 11/83	TITLE ASSY, HEAD / DISK WIDGET
ENG APPVL 11/83; MFG APPVL	
RELEASE 11/83; ORIG DIV M.S.D.	
DESIGNER; SCALE FULL	SIZE D; DRAWING NUMBER 677-6000-A; SHT 1/2

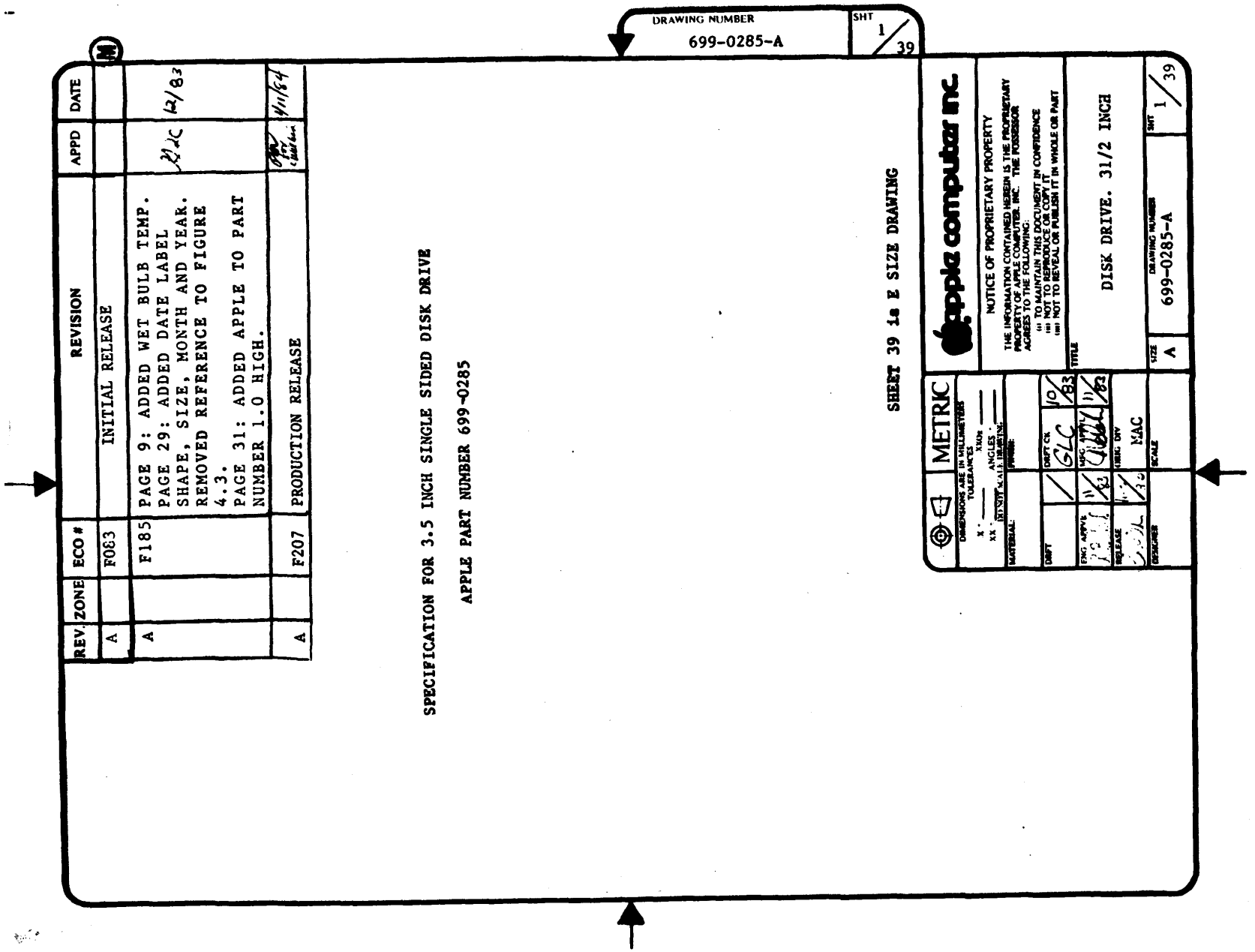
"APPLE_677-6000-A-1of2.PICT" 822 KB 2002-03-12 dpi: 200h x 200v pix: 8684h x 5657v



"APPLE_677-6000-A-2of2.PICT" 462 KB 2002-03-12 dpi: 200h x 200v pix: 8702h x 5661v



"APPLE_699-0165-A-1of1.PICT" 3164 KB 2002-03-12 dpi: 200h x 200v pix: 12854h x 8244v



"APPLE_699-0285-A-01of39.PICT" 193 KB 2002-03-12 dpi: 200h x 200v pix: 3282h x 2547v

CONTENTS

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SIZE	DRAWING NUMBER
A	699-0285-A
SCALE:	SHEET 2 OF 39

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SIZE	DRAWING NUMBER
A	699-0285-A
SCALE:	SHEET 3 OF 39

apple computer inc.

SIZE	DRAWING NUMBER
A	699-0285-A
SCALE:	SHEET 4 OF 39

1.0 Description

This specification defines a single sided 3.5 inch Micro-Floppy disk Drive, Apple part number 699-0285.

2.0 Specification

The drive shall satisfy the following specifications when a diskette meeting the Apple disk specification, specification number 003-0001, is used.

2.1 Configuration

The drive consists of a read/write head, head positioning mechanism, disk motor, interface logic circuit, read/ write circuit, and auto eject, and uses a 3.5 inch microfloppy diskette, as shown in Figure 2.1. The drive itself shall meet UL 478 and CSA C22.2 No. 154-1983 requirements for safety.

2.2 Mechanical Dimensions

The mounting holes are shown in Figure 2.2, and the complete mechanical dimensions are shown in Apple drawing number 699-0285 page 39, which is an addendum to this specification available on request.

2.3 Performance

2.3.1 Capacity and Encoding Method - see Appendix B

2.3.2 Transfer Rate

Detected flux transistions shall occur not less than 1.89 usec nor more than 6.36 usec apart.

2.3.3 Access Time

a. Track to track slew rate : 12 msec Max
b. Track to track step settling time : 30 msec Max
(These times are satisfied when the head is positioned and stable within 0.035 mm of its absolute position as defined in 2.11.)

c. Speed group to speed group motor settling time : 150 msec Max
d. Motor start time : 400 msec Max
(These times are satisfied when the motor speed has settled to within +/- 1% of its final average rpm.)

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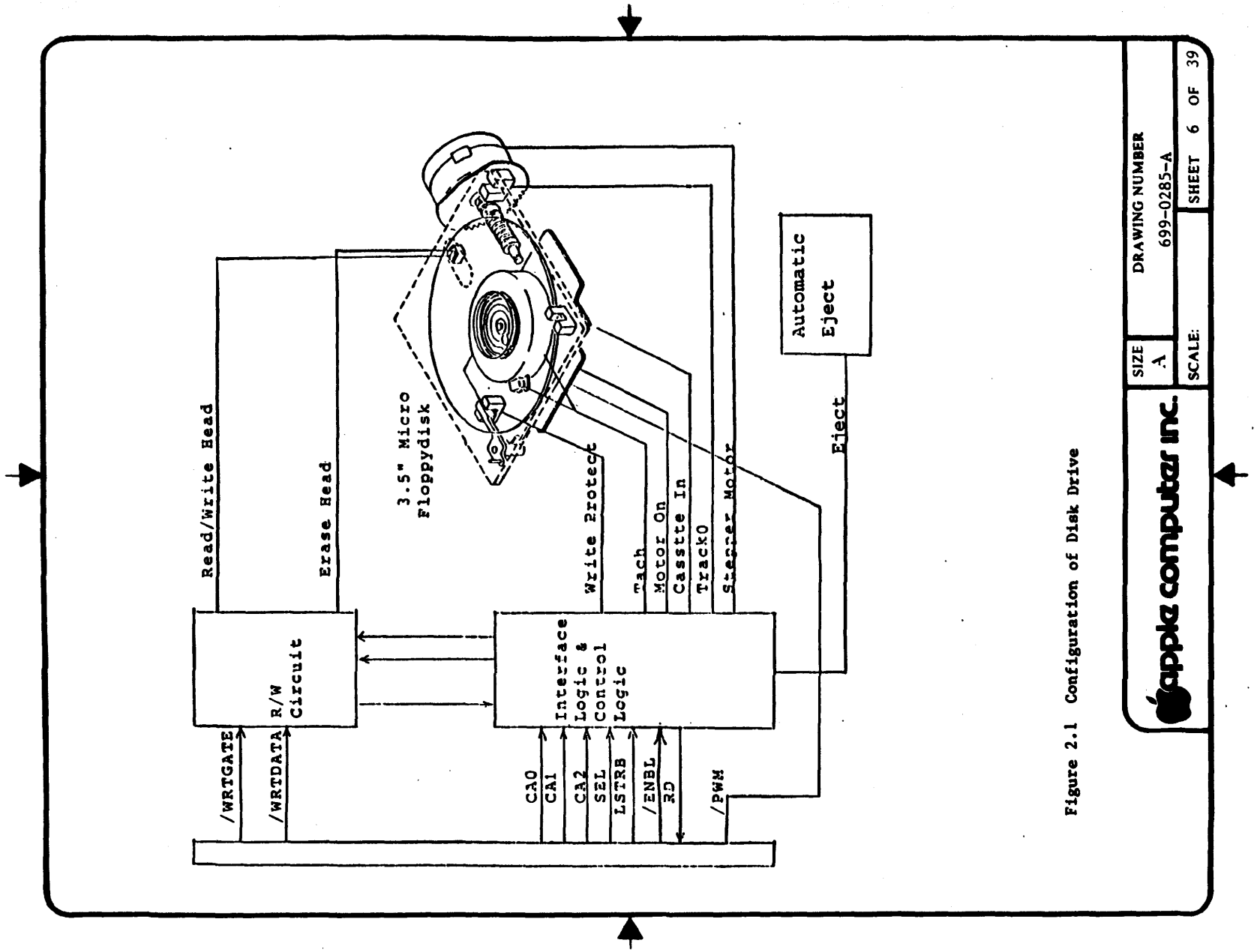

Figure 2.1 Configuration of Disk Drive

"APPLE_699-0285-A-06of39.PICT" 189 KB 2002-03-12 dpi: 200h x 200v pix: 3300h x 2527v

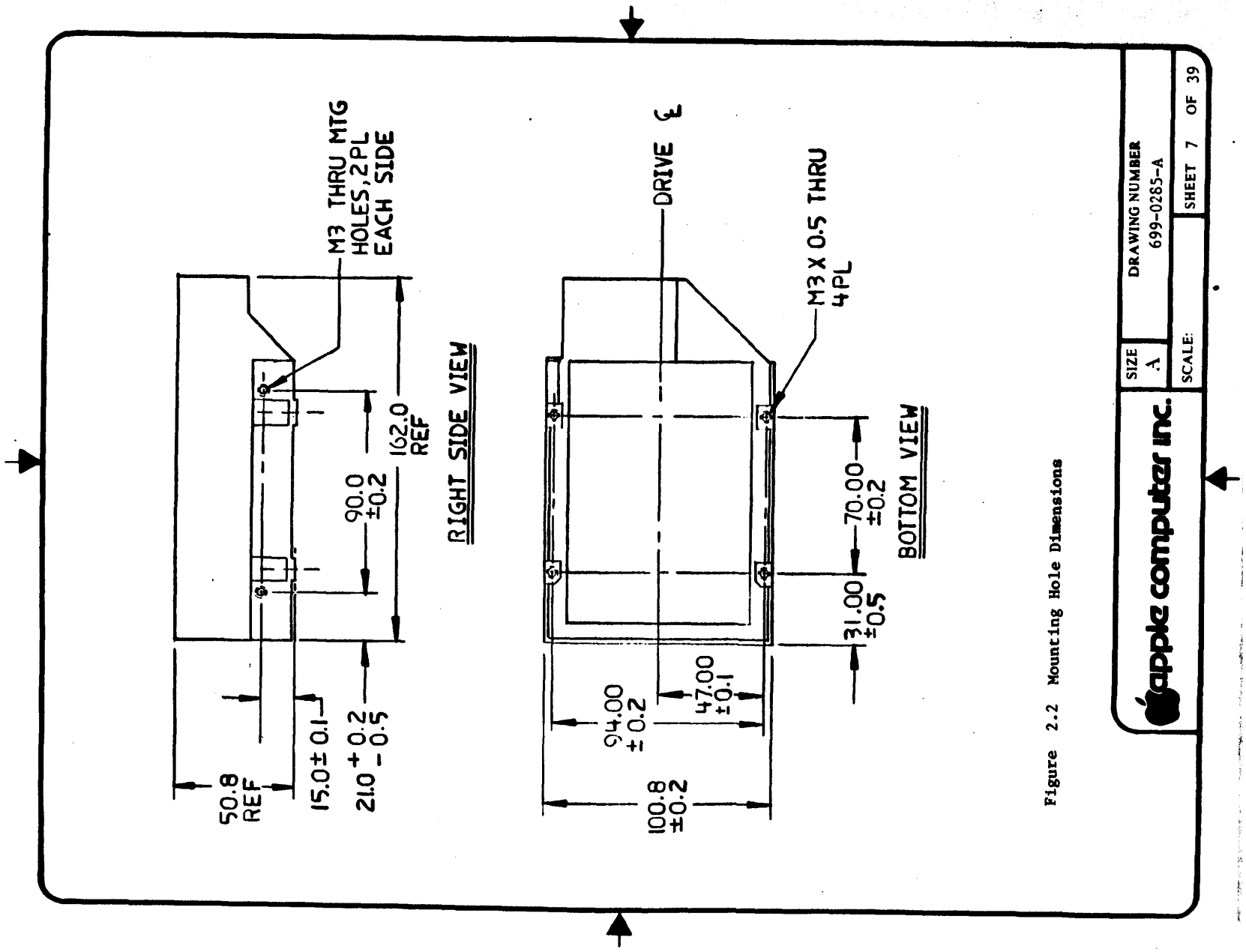

Figure 2.2 Mounting Hole Dimensions

2.3.4 Functional

a. Rotational Speed:

The motor speed is variable to allow recording to be done at fixed density as the head moves from the outer edge of the diskette toward the center. The speed is continuously variable from 390 to 605 rpm using a pulse width modulated signal input.

The detailed specifications on disk motor speed are given in 2.17.

b. Recording Density

The maximum recording density assumes all 2 usec transistions while the minumum density assumes all 6 usec transistions even though the format doesn't allow more than one 6 usec interval to be written at a time.

Maximum	:	8472 FCI
Minimum	:	2365 FCI

c. Track Density : 0.1875mm Track - Track

d. Tracks : 80

e. R/W Head : 1

2.3.5 Weight: 750g Max

2.4 Input Power Requirements

Voltage	Max. Ripple	Current
+12.0V +/-5%	0.1Vpp	Standby 0.15A (motor off) Average 0.3A (motor on) Peak 1.0A (stepping)
+5.0V +/-5%	0.1Vpp	0.5A maximum

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2.5 Environmental limits

2.5.1 Temperature

Operating : 5 C to 50 C (40 F to 122 F) ambient

Non-Operating: -40 C to 60 C (-40 F to 140 F)
The temperature cycling shall not result in condensation.

2.5.2 Humidity

Operating : 20% to 80% relative humidity with a wet bulb temperature of 29 C (85 F), with no condensation.

5% to 90% relative humidity with a wet bulb temperature of 37.8 C (100 F) if the track alignment specification (Section 2.11) is relaxed to +/-0.040 mm from +/-0.035 mm, with no condensation.

Non-Operating: 5% to 95% relative humidity with no condensation.

2.5.3 Vibration

Operating : The unit shall perform read/write operation without errors with continuous vibration from 5 to 100 Hz at a maximun of 0.5G along each of the three mutually perpendicular axes.

Non-Operating: The unit shall be able to withstand continuous vibration from 5Hz to 300Hz with a maximun level of 2.0G along each of the three mutually perpendicular axes without any degradation of any characteristics below the performance specification.

2.5.4 Shock

Operating : The unit shall be able to withstand a 1.0G shock for 11 milliseconds with a 1/2 sine wave shape in each of the three mutually perpendicular axis while performing normal read/write functions without damage or any loss of data.

Non-Operating: The unit when unpacked shall withstand a shock of 60G on any of the three mutually perpendicular axis.

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2.6 Noise

Operating : Noise from the drive shall be less than 55 Dba at a point 50cm from the drive.

2.7 Orientation

The drive may be used in the three orientations shown in Figure 2.3.

2.8 Reliability

a. Mean Time Between Failure (MTBF): 8000POH
b. Mean Time to Repair (MTTR) : 30 minutes
c. Preventive Maintenance (PM) : Not Required
d. Component life : 5 years
e. Error Rate

1. Soft Read : 1 per 10^{9} bits read
2. Hard Read : 1 per 10^{12} bits read
3. Seek Error : 1 per 10^{6} seeks

2.9 Overwrite Characteristics

The residual level of 1F (125 KHz) measured as follows shall be greater than 30 db.

To measure, first record the 1F signal on TK0, then write over the track once with a 2F (250 KHz) signal, and measure the residual level of 1F at the read head.

Residual signal level ratio (db):

2F signal level (db) - residual level of 1F (db)

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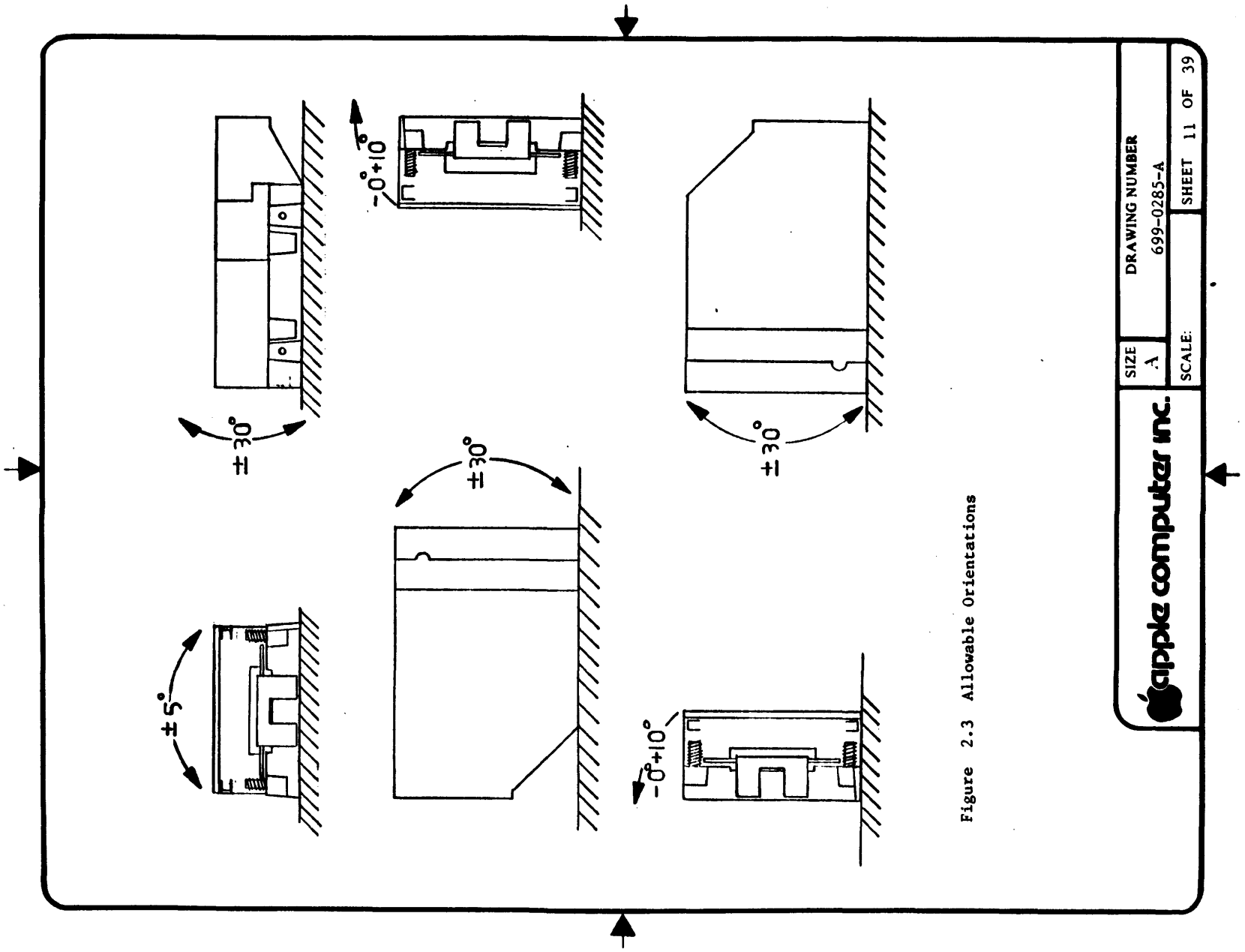

Figure 2.3 Allowable Orientations

2.10 Time Margin

2.10.1 Definition of time margin

Time margin is measured using the Apple jitter generating fixture. This circuit jitters the read pulse coming from the drive under test randomly. The time margin is defined as the largest value of time that the read pulse can be jittered while still allowing the controller to read with fewer than one error in ten million bits read. The schematic of the jitter generator, Apple part number 890-2002, is shown in Appendix A.

The data read is comprised of a random pattern of flux changes including all legal combinations of 2, 4, & 6 usec periods between flux changes.

Track format and Sector format is defined in Appendix B.

2.10.2 Self read/write time margin

The self read/write time margin shall be: >300 nS

2.10.3 Off-track Time Margin

The time margin using a reference disk on which random data is written +0.035 mm and -0.035 mm off track shall be >300 ns.

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2.11 Alignment Accuracy

Track position is defined by:

RN = 39.5 — 0.1875 x N

Where RN: Absolute track position from disk center
N: Track number from 0 to 79

Alignment Accuracy at track 40 shall be: +/-0.020 mm

Alignment Accuracy at all other tracks shall be: +/-0.035 mm

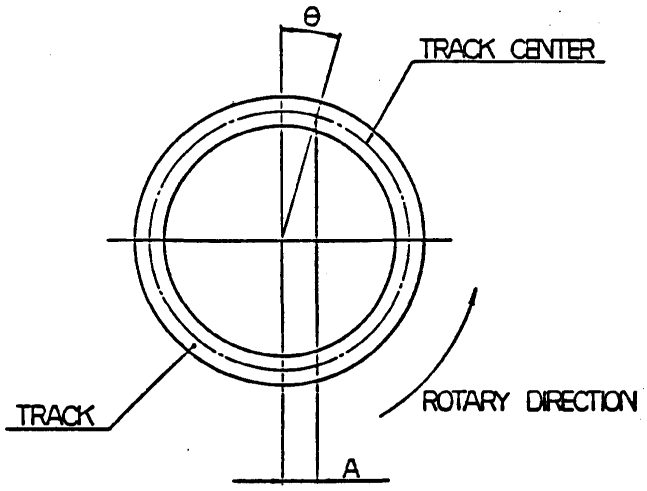
2.12 Azimuth Angle

Azimuth Angle shall be;

Angle = arcsin (0.35 / (X - YN)) +/- 0 degrees 30'

where : X = 39.5
Y = 0.1875
N = Track number (0 to 79)

Azimuth angle is defined in Figure 2.4.



SIDE 0 VIEW

Figure 2.4 Azimuth Angle

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2.13 Off Track Error Rate

a. Using the plus-off-tracked disk on which random flux transistions are recorded off-track +35um from the reference position on all tracks, the drive shall meet the error rate specification.

b. Using the minus-off-tracked disk on which random flux transistions recorded off-track -35um from the reference position on all tracks, the drive shall meet the error rate specification.

2.14 Temperature Inside Drive

The temperature rise above ambient at the disk surface inside of the drive shall not exceed 10 degrees C when the drive is used at 50% duty cycle Random Seek with random reads and writes. The drive shall be set in free air at an ambient temperature of 50 degrees C maximum.

2.15 Head Life

Head life shall be more than (20,000,000) passes. Measured as follows:

a. Using a new disk, which is used as the reference disk for signal level, and a new drive, move the head to Track 35, then record 2F signal. Measure the output signal level (Lr).

b. Insert another new disk into the drive. Move the head from Track 0 to Track 79 and back to Track 0 about 3,000,000 passes.

c. Change the disk to another new disk.

d. Repeat (b) and (c) until total number of passes is 20,000,000.

e. Change the disk to the reference level disk used in (a). Move the head to Track 35, measure the output signal level (Lx).

f. The ratio of Lx over Lr shall be > 80% as follows:

$$\frac{Lx}{Lr} \times 100\% > 80\%$$

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2.16 Media Wear

Write the 2F signal on every track of a new disk, and read the output level of all of the tracks and record. After 3,000,000 read passes on track 35, the output level of all tracks should be 80% minimum of the originally measured value of each track.

2.17 Disk Motor

The disk motor speed shall be controlled by a PWM signal from the host computer. The specifications of the disk motor are as follows:

2.17.1 Speed Control Range

a. Speed at 9.4% duty cycle of PWM with the diskette in place and head at TK0 (measured at 25 +/- 3 degrees C) shall be:

$$305 < V_{low} < 380\text{rpm}$$

b. Speed at 91% duty cycle of PWM with diskette in place and head at TK79 (measured at 25 +/- 3 degrees C) shall be:

$$625 < V_{high} < 780\text{rpm}$$

c. Over the full environmental range as specified in Section 2.5, and with a diskette in place the following speeds must be guaranteed including all jitter and drift effects:

With the head positioned at TK0 and the PWM set to 9.4%, the motor speed must be less than 390 rpm.

With the head positioned at TK79 and the PWM set to 91%, the motor speed must be greater than 605 rpm.

2.17.2 Linearity

Non-linearity of the disk motor speed shall be less than 2.0%.

Linearity is defined as,

$$\text{Linearity} = \left| \frac{Vx - Vr}{Vr} \right| \times 100\%$$

where :

$$Vr = \frac{(Va - Vb)}{81.6} (x - 9.4) + Vb$$

Vx : Measured speed at a PWM duty cycle of x %.
Va : Measured speed at a PWM duty cycle of 91%.
Vb : Measured speed at a PWM duty cycle of 9.4%.

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2.17.3 Jitter

Jitter of the disk motor speed shall be less than 1.8% peak - peak when measured at a motor speed of between 390 and 605 RPM. Jitter is defined as:

$$\text{Jitter} = \frac{4\ Sx}{Sm} \times 100\%$$

where : Sx is the standard deviation of the TACH pulse period sampled randomly 100 points and Sm is the mean of Tach pulse period.

2.17.4 Thermal drift

Thermal drift of disk motor speed for any speed between 390 and 605 rpm shall be less than 3%. The definition of the thermal drift:

$$\text{Thermal drift} = \left| \frac{Vx - Vr}{Vr} \right| \times 100\%$$

where : Vr : Disk motor speed at 25 C ambient temperature.

Vx : Disk motor speed between 5 C to 50 C ambient temperature.

2.17.5 Initial drift

Initial drift of disk motor speed shall be less than 1.0%. Initial drift is defined as:

$$\text{Initial drift} = \left| \frac{Vx - Vr}{Vr} \right| \times 100\%$$

where : Vr : Disk motor speed at 1 sec after disk motor is turned on.

Vx : Disk motor speed at 120 sec after disk motor is turned on.

2.17.6 Speed - Torque characteristics

The change of speed with torque is:

Ratio of speed/torque : -0.25% /gram cm

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2.18 Eject Mechanism

2.18.1 Eject Timing

From the leading edge of the eject signal which is 750 +/- 25 milliseconds in duration, the total eject time shall be less than 1.5 seconds. Note that the "cassette in" signal is not guaranteed to indicate no cassette in place until the eject operation is complete.

2.18.2 Eject Mechanism Life

The eject mechanism shall be capable of at least 20,000 disk insertions and ejections using the auto eject mechanism without degradation of specifications or failure. Both insertion and ejection shall be smooth and quiet.

2.18.3 Manual Eject

A mechanism shall be provided which allows manual eject of the diskette. The maximum pressure necessary to eject the diskette using this mechanism shall be 1.3 Kg.

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3.0 Interface

3.1 General Description

The interface between the host system and the drive consists of 6 input signals (SEL, CA2, CA1, CA0, /ENBL, and LSTRB) and one output signal (RD). For any communication with the drive, the /ENBL line must be low.

3.1.1 Reading Status or Data from Drive.

The host system can read the status of the drive or data on the disk using the RD line by setting the CA0, CA1, CA2 and SEL signals as shown in the table (the RD line is a tristate line which is in the high impedance state unless /ENBL is low).

SEL	CA2	CA1	CA0	Output signal on RD line
0	0	0	0	/DIRTN
0	0	0	1	/STEP
0	0	1	0	/MOTORON
0	0	1	1	(EJECT)
0	1	0	0	RDDATA (Head0)
0	1	1	0	SIDES
0	1	1	1	/DRVIN
1	0	0	0	/CSTIN
1	0	0	1	/WRTROT
1	0	1	0	/TK0
1	0	1	1	/TACH
1	1	0	0	RDDATA (Head1)
1	1	1	0	Reserved
1	1	1	1	Reserved

3.1.2 Sending Control Commands to Drive.

The host system can send four commands: /DIRTN, /STEP, /MOTORON and EJECT. To send one of the control commands to the drive, set CA2 to the value (a zero or a one) to which the host system wishes the command to be set, and then set CA0, CA1 and SEL to the value which selects the desired command. Finally, bring LSTRB first high and then low.

Note 1: EJECT is an unlached output only: EJECT is a signal which cannot be read (it always reads the value one). To eject a disk, set SEL, CA2, CA1 and CA0 as 0111, then hold LSTRB high for 750 msec.

Note 2: CA0, CA1, CA2 and SEL must not change value while LSTRB is high and CA0 and CA1 must be returned to a one level before changing SEL.

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3.2 Signal Descriptions

3.2.1 /CSTIN

This signal goes to a zero only when a disk is in the drive.

3.2.2 /WRTPRT

This signal goes to a zero only when a write-protected disk is in the drive, or when no disk is in the drive.

3.2.3 /TK0

This signal goes to a zero only when the head is located at track 0. From the time the /STEP signal is set to a zero, a delay of 12msec is required before TK0 is valid.

3.2.4 /TACH

This signal is used to monitor the disk motor speed. /TACH signal specification is as follows:

Number of pulses per rotation	: 60
Duty cycle	: 50% +/- 10%
Accuracy of pulse period	: +/- 0.2%

3.2.5 /DIRTN

This signal sets the direction of head motion for stepping from one track to another. A zero sets the direction towards the center of the disk. A one sets the direction towards the outer edge of the disk. When the drive is disabled (/ENBL high), /DIRTN is set to a zero.

3.2.6 /STEP

At falling edge of this signal, the head starts to move to the adjacent track. When the step sequence is complete, /STEP is set to a one by the drive. The direction is determined by /DIRTN. When the drive is disabled (/ENBL high), /STEP is set to a one.

3.2.7 /MOTORON

When this signal is set low, the disk motor is turned on if a disk is in the drive. When the drive is disabled (/ENBL high), /MOTORON is set to a one.

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3.2.8 EJECT

Setting EJECT to a one causes the disk to be ejected from the drive. The EJECT must be a one for 750 msec +/-25 msec to eject a disk. When the drive is disabled (/ENBL high), the EJECT is set to a zero.

3.2.9 SIDES

This status bit is read as a zero if the drive is single-sided, or a one if the drive is double-sided.

3.2.10 /DRVIN

This status bit is read as a zero only if the selected drive is actually connected to the host system.

3.2.11 RDDATA

RDDATA is the actual data read from the disk.

3.2.12 /PWM

The /PWM signal is used by the host computer to adjust the speed of the drive motor. This TTL level signal transmits timing information in the form of a fixed pulse rate of from 20 KHz to 40 KHz. The duty cycle of each pulse is defined as the percentage of time the signal is at a logic zero level. The disk motor speed control is specified to operate at the correct speed for duty cycles between 10% and 90%. One implementation of the speed control uses a PWM rate of 22 KHz, and gains extra resolution by "dithering" the pulse duty cycle such that each set of 10 successive pulses varies in duty cycle. This method increases the resolution by a factor of 10 but also results in decreasing the effective frequency of the control signal to 2.2 KHz.

3.2.13 CA0, CA1, CA2, SEL

These signals are used to multiplex inputs from the drive to the RD line during a read operation. During a command write operation these signals select addressable latches in the drive (except for EJECT). CA2 serves the special purpose of selecting a one or a zero to be set into the addressable latches during a write. SEL is used as "Head Select" for a double sided drive during a read.

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3.2.14 /ENBL

This line enables all communication with the drive. When /ENBL is high (drive disabled), the RD output goes into a high impedance state, and the control latches in the drive are preset to their inactive states.

3.2.15 LSTRB

This line is used to send a command to the drive. After setting CA0, CA1, CA2 and SEL to the desired state, LSTRB is brought first high and then low.

3.2.16 RD

This line is the only output line from the drive. It is multiplexed by the control lines and allows the host to read disk status information as well as data.

3.2.17 WRTDATA

This line is used for data that is to be written on the disk. The magnetized pattern on the disk is same as the level of WRTDATA. Each change in the level of WRTDATA causes a flux transistion to be written on the disk. WRTDATA is allowed to record on the disk only when /WRTGATE is a zero.

3.2.18 /WRTGATE

This signal enables data to be written on the disk and turns on the erase head.

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3.3 DC Characteristics of Interface Signals

3.3.1 Output Drive

Name	Output Current (milliamps) IOH	IOL	Output Voltage (volts) VOH	VOL
RD*	-1.0	6.5	2.4	0.5

3.3.2 Input Loading

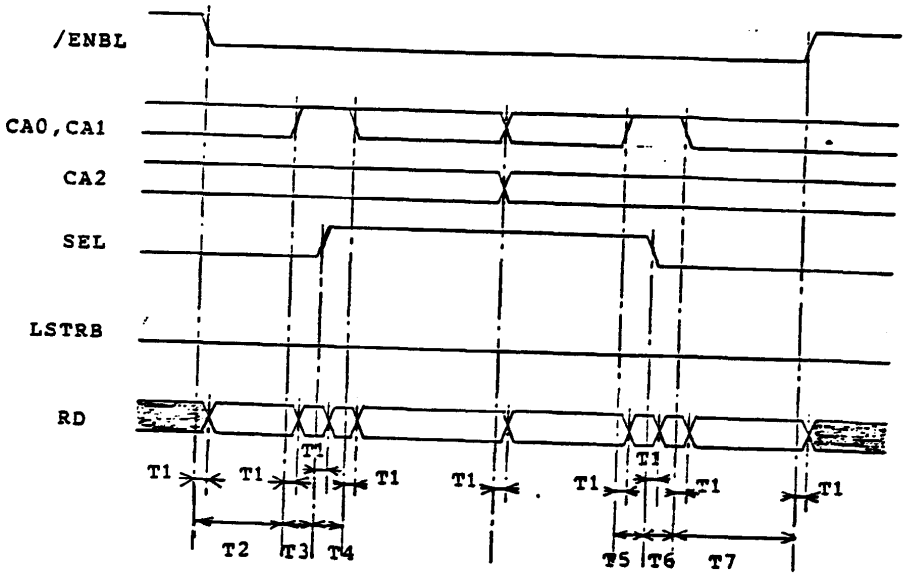
Name	Input Current (milliamps) VIN=2.4V IIH	VIN=0.4V IIL	Input Voltage threshold (volts) VIH	VIL
WRTDATA*, /WRTGATE*	-0.9	-1.5	2.0	0.8
CA0-CA2, LSTRB, SEL	0.1	-0.25	2.0	0.8
/ENBL	0.125	-0.75	2.2	0.8
/PWM	0.01	-0.04	2.0	0.8

*These signal lines include a 3.3K pull-up resistor to +5v.

3.4 Timing Requirements

The following sections contain timing diagrams which show the relationship between the input and output signals.

3.4.1 Reading one of the status signals



T1 : 0.5 us Max
T2 : 0.5 us Min
T3 : 0.5 us Min
T4 : 0.5 us Min
T5 : 0.5 us Min
T6 : 0.5 us Min
T7 : 1 us Min

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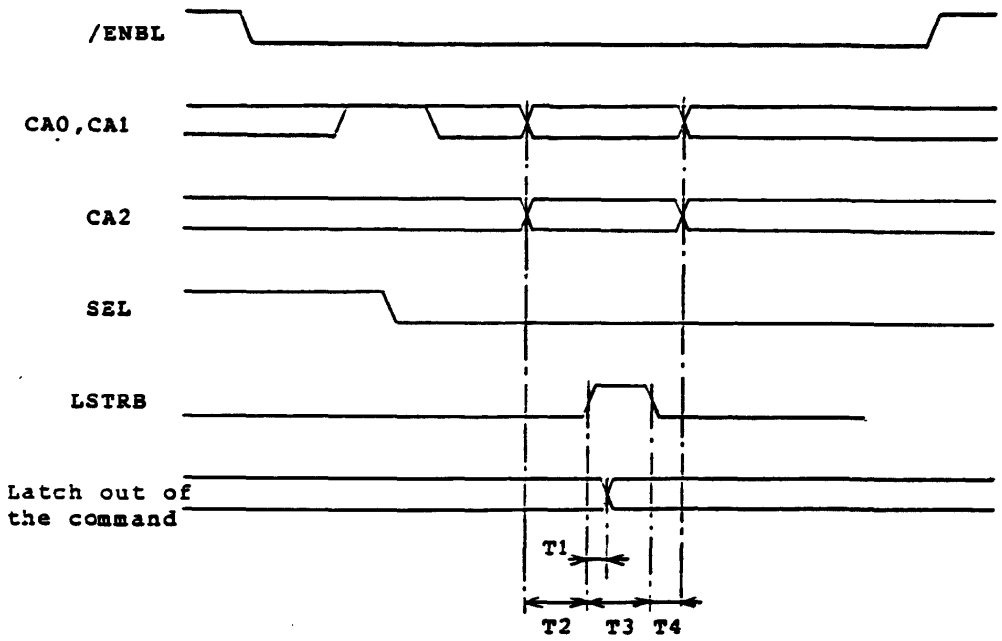
3.4.2 Sending one of the control commands



T1 : 1 us
T2 : 0.5 us
T3 : 1 us Min except for EJECT
0.75 s for EJECT
T4 : 0.5 us

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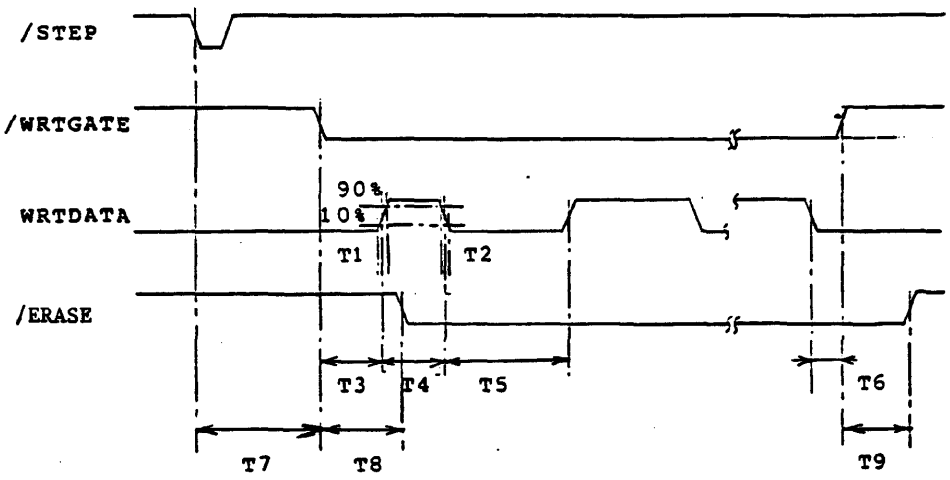
3.4.3 /WRTGATE, WRTDATA and /ERASE Timing



T1 : 100 ns Max
T2 : 100 ns Max
T3 : 1.8 us
T4 : 2 us +/- 0.05 us for 2 usec period*
: 4 us +/- 0.05 us for 4 usec period*
: 6 us +/- 0.05 us for 6 usec period*
T5 : 2 us -/+ 0.05 us for 2 usec period*
: 4 us -/+ 0.05 us for 4 usec period*
: 6 us -/+ 0.05 us for 6 usec period*
T6 : 2us
T7 : 12 ms + 30 ms Min
T8 : 250 us +/- 6 us
T9 : 884 us +/- 5 us

*These numbers will be different if the system clock frequency is different, however, since the disk controller controls both read and write frequency, no decrease in time margin is experienced due to this effect. For disks recorded on different systems to be interchangeable, the data density on the disk must be the same.

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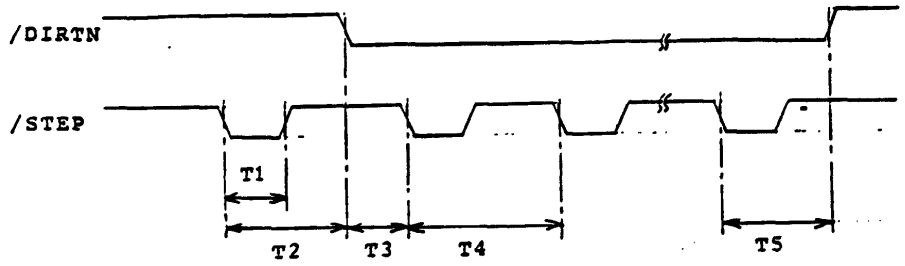
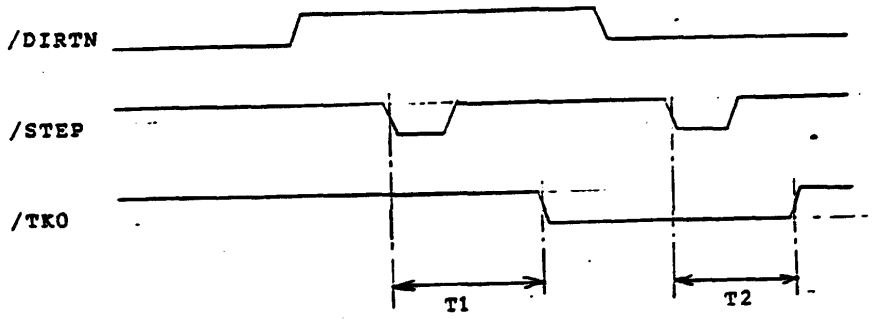
3.4.4 /DIRTN and /STEP Timing



T1 : 10 us Min 12 ms Max
T2 : 10 ms Min
T3 : 2 us Min
T4 : 12 ms Min
T5 : 11 us Min

3.4.5 /TKO Timing



T1 : 12 ms Max
T2 : 12 ms Max

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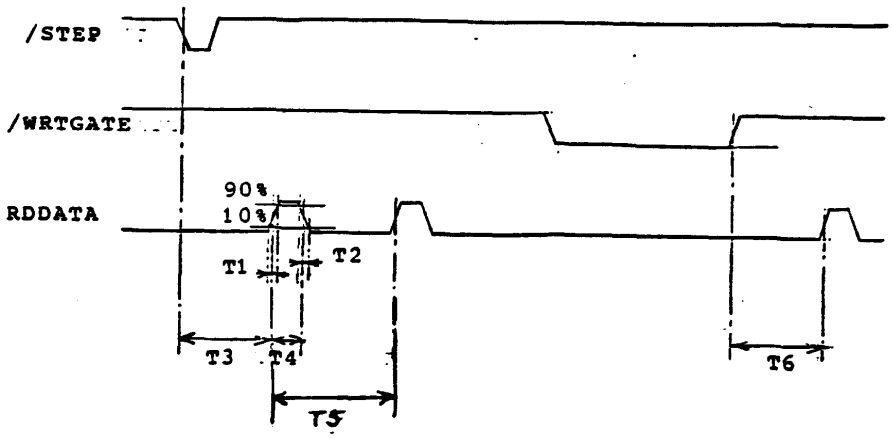
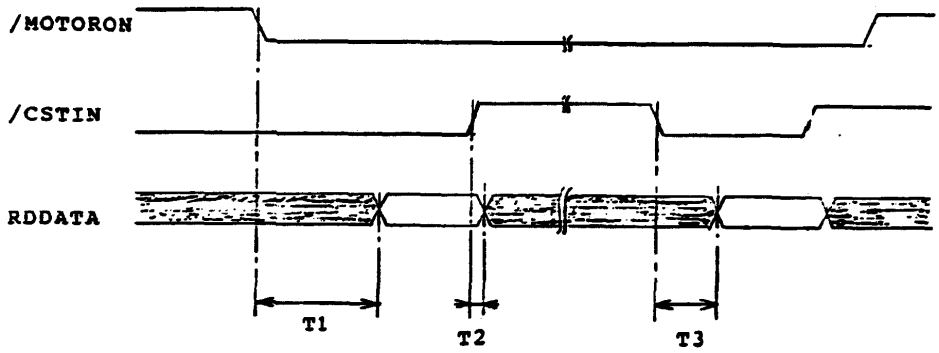
3.4.6 RDDATA VALID TIMING - CONDITION 1



T1 : 100 ns Max
T2 : 100 ns Max
T3 : 12 ms STEP + 30 ms HEAD SETTLING
T4 : 400 ns Min 800 ns Max
T5 : 2 us, 4 us, or 6 us
T6 : 10 us (data error may occur when ERASE goes off)

3.4.7 RDDATA VALID TIMING - CONDITION 2



T1 : 400 ms Max
T2 : No Requirement
T3 : 1 second Max

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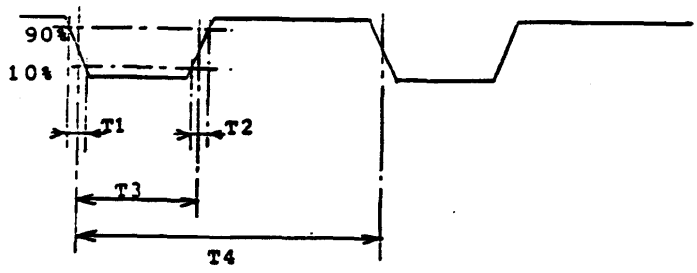
3.4.8 /PWM WAVEFORM



T1 : 50 ns
T2 : 50 ns
T3 : 10% to 90% of T4
T4 : 25 us to 50 us

3.5 Power On and Power Off Requirements

3.5.1 Data Protection

There shall be no damage to recorded data on the disk during either a power on or power off operation as long as the disk is not in the middle of a write when power is turned off.

3.5.2 Power Supply Sequencing

No special power supply sequencing shall be required by the disk as long as both the +5 volt and +12 volt power supplies have a monotonic rise time of less than 100 milliseconds. That is there shall be no ringing on the supplies during turn on or turn off which causes them to rise above and then fall below their specified voltage. Some ringing is tolerable as long as it doesn't cause the voltage to exceed or fall below the specified limits (+/-5%).

At turn off, both supplies must fall monotonically to zero volts, however, there are no sequencing or timing requirements.

3.5.3 Head Position Initialization

At power on, the head shall be automatically accessed to track 0.

3.6 Interface Connector and Pin Assignment

The interface connector shall be a 20 pin connector, 3M J3428-5202 or equivalent. The pinouts are as follows:

Pin number	Signal Name	Pin Number	Signal Name
1	GND	2	CA0
3	GND	4	CA1
5	GND	6	CA2
7	GND	8	LSTRB
9	N/C	10	/WRTGATE
11	+5V	12	SEL
13	+12V	14	/ENBL
15	+12V	16	RD
17	+12V	18	WRTDATA
19	+12V	20	/PWM

4.0 Labelling

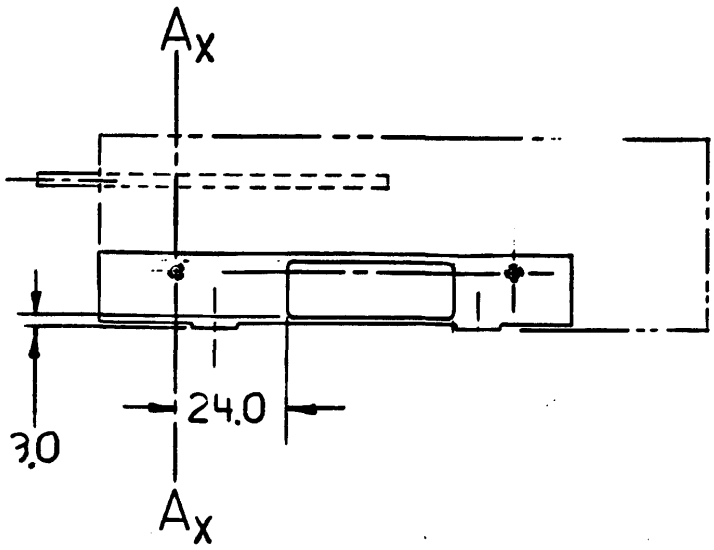
The drive shall have two labels attached when it is shipped to Apple.

4.1 Label Position

The serial number label shall be attached to the right side, and the date label to the left side of the chassis as shown in Figure 4.1.

4.2 Label Contents

The shape and contents of the serial number label shall be as shown in Figure 4.2. The date label shape and size may be picked by the drive manufacturer, but must include the month and year of manufacture and be clearly legible.

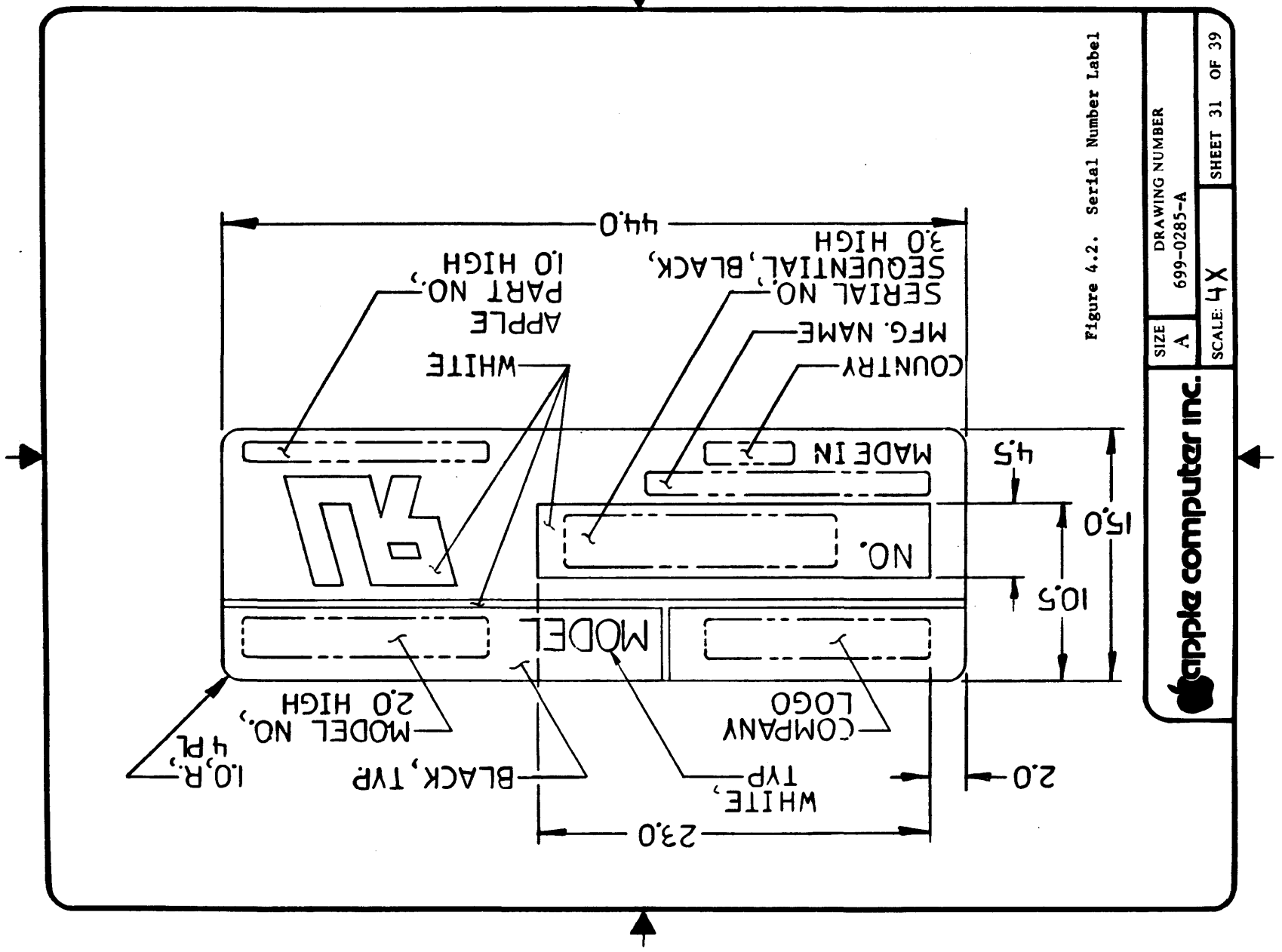


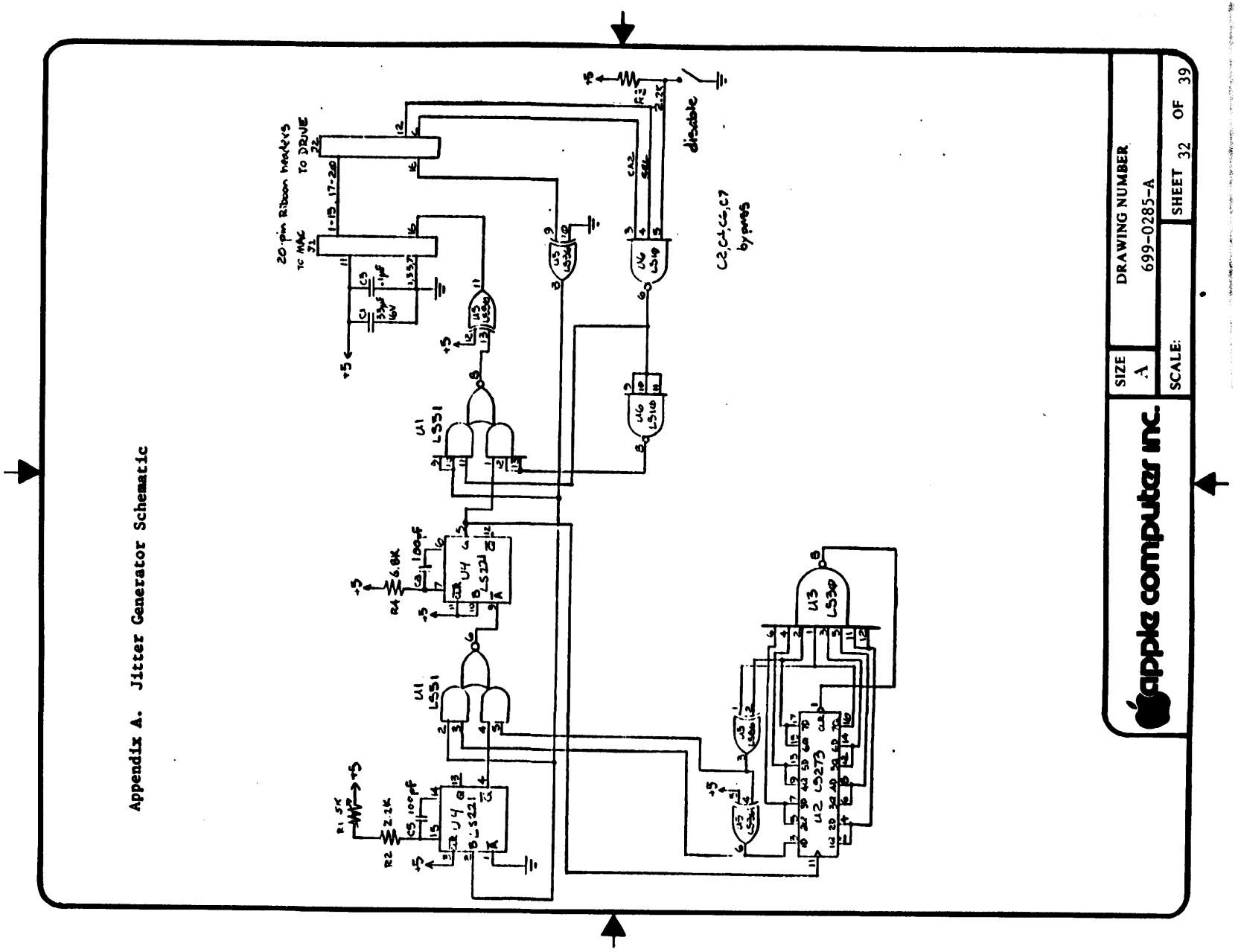
SCALE : NONE

TOL. : XX.X ±0.4

Figure 4.1 Label Position

apple computer inc.	SIZE A	DRAWING NUMBER 699-0285-A
	SCALE:	SHEET 30 OF 39


44.0
3.0 HIGH
SEQUENTIAL, BLACK,
SERIAL NO.,
1.0 HIGH
PART NO.,
APPLE
WHITE
MFG. NAME
COUNTRY
MADE IN
4.5
15.0
10.5
NO.
MODEL
2.0 HIGH
MODEL NO.,
1.0 R.,
4 PL
BLACK, TYP
COMPANY
LOGO
WHITE,
TYP
2.0
23.0
Figure 4.2. Serial Number Label
SIZE A
DRAWING NUMBER 699-0285-A
SCALE: 4X
SHEET 31 OF 39
apple computer inc.

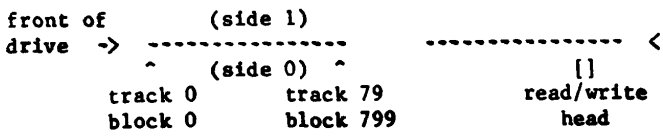


"APPLE_699-0285-A-32of39.PICT" 179 KB 2002-03-12 dpi: 200h x 200v pix: 3300h x 2546v

Appendix B. Sector Format

This document describes the sector format used for single-sided 3-1/2 inch diskettes; provision is made for eventual expansion to double-sided diskettes.

The current drive has a single read/write head located on the bottom of the drive at the back (the diagram below shows a side-view of a drive, the dotted line representing a diskette):



There are 80 tracks on the drive, numbered from track 0 (the outermost track) through track 79 (the innermost track). The single side is side 0: the top side, side 1, will be used on future double-sided disk drives.

The number of sectors per track varies from 12 on the outside tracks to 8 on the inside tracks as shown in the following table. Speed 1 represents a data transfer rate of 489.6 K bits/sec. Speed 2 is for 500 K bits/sec. The different speeds record the data at a fixed density and allow the diskettes to be interchanged.

Track	Speed Group	Sectors/Track	Speed 1	Speed 2
0 - 15	1	12	394	402
16 - 31	2	11	429	438
32 - 47	3	10	472	482
48 - 63	4	9	525	536
64 - 79	5	8	590	603

This format is derived by limiting the sectors per track for the single-sided drive according to the smaller radius of the opposite-side track of the future double-sided drive. This format yields a total of 800 sectors or blocks. Block numbering goes from 0 to 799: block 0 is sector 0 on track 0 and block 799 is sector 7 on track 79 (sectors are numbered from 0). Future double-sided disks will have an additional 800 blocks on side 1; these blocks will be interleaved with side 0 blocks in a cylinder fashion (blocks 0-11 will be on side 0, track 0, blocks 12-23 will be on side 1, track 0, etc.).

Sectors are typically interleaved 2:1 because of the write recovery time. As an example, the sector sequencing for 2:1 interleave is:

speed group 1: 0-6-1-7-2-8-3-9-4-10-5-11
speed group 2: 0-6-1-7-2-8-3-9-4-10-5
speed group 3: 0-5-1-6-2-7-3-8-4-9
speed group 4: 0-5-1-6-2-7-3-8-4
speed group 5: 0-4-1-5-2-6-3-7

apple computer inc.

SIZE	DRAWING NUMBER
A	699-0285-A
SCALE:	SHEET 33 OF 39

Sector Format

A sector can be divided into four major sections. These are the header sync field, the header field, the data sync field, and the data field. These fields combined add up to 733.5 code bytes minimum.

Header Sync Field (6.25 bytes + sync overhead)

5 bit slip FFs minimum (FF,3F,CF,F3,FC,FF)

The header sync field contains a pattern of ones and zeroes that synchronizes the hardware state machine with the data on the disk. The header sync and header fields are written only when the diskette is formatted. The formatter should make this field as large as possible since this field buffers expansion of the previous sector's data field due to speed variation of the drive.

Header Field (11 bytes)

D5 AA 96 Trk Sect Side Fmt ChkSum DE AA off

The header field identifies the sector. The sub-fields are:

D5 AA 96	address marks: this identifies the field as a header field.
Track	encoded low 6 bits of track number
Sector	encoded sector number
Side	encoded high 2 bits of track number and side bit: decoded bit 5 = 0 for side 0, 1 for side 1 decoded bit 0 is the high-order bit of the track number decoded bits 1-4 are reserved and should be 0
Format	encoded format specification: decoded bit 5 = 0 for single-sided formats decoded bits 0-4 define the format interleave: standard 2:1 interleave formats have a 2 in this field
Checksum	checksum formed by exclusive 'or'ing the track, sector, side, and format fields
DE AA	bit slip marks: this identifies the end of the field
off	pad byte where the write electronics were turned off

Data Sync Field (6.25 bytes)

5 bit slip FFs (FF,3F,CF,F3,FC,FF)

The data sync field contains a pattern of ones and zeroes that synchronizes the state machine with the data on the disk. This field is written whenever the data field is written.

apple computer inc.	SIZE A	DRAWING NUMBER 699-0285-A
	SCALE:	SHEET 34 OF 39

Data Field (710 bytes)

```
-----------------------------------------
D5 AA AD Sect <encoded data> ChkSum DE AA off
-----------------------------------------
```

The data field contains the actual data in the sector. The sub-fields are:

D5 AA AD	**data marks: this identifies the field as a data field.**
Sector	**encoded sector number**
encoded data	**524 data bytes encoded into 699 code bytes; the first 12 data bytes are typically used as a sector tag by the operating system, and the remaining 512 bytes for actual data**
Checksum	**a 24-bit checksum encoded into 4 code bytes (see below)**
DE AA	**bit slip marks: this identifies the end of the field**
off	**pad byte where the write electronics were turned off**

Data Encoding Format

A sector is composed of 524 user data bytes and a 3 byte checksum. These are translated into 6 bit nibbles that are used to look up GCR codewords to be written to the disk. The data is encoded as follows. CSUMA, CSUMB,CSUMC are registers used for accumulating the checksum. BYTEA, BYTEB, BYTEC contain three bytes from the data buffer. GCR is the table of GCR codewords.

1. Rotate CSUMC left
   CSUMC[76543210] <- CSUMC[65432107]
   Carry <- CSUMC[7]
2. CSUMA <- CSUMA + BYTEA + carry from step 1
3. BYTEA <- BYTEA xor CSUMC
4. CSUMB <- CSUMB + BYTEB + carry from step 2
5. BYTEB <- BYTEB xor CSUMA
6. CSUMC <- CSUMC + BYTEC + carry from step 4
7. BYTEC <- BYTEC xor CSUMB
8. Convert BYTEA, BYTEB and BYTEC to 6 bit nibbles
   NIBL1 <- A7 A6 B7 B6 C7 C6 High bits of the bytes
   NIBL2 <- A5 A4 A3 A2 A1 A0 Low bits of BYTEA
   NIBL3 <- B5 B4 B3 B2 B1 B0 Low bits of BYTEB
   NIBL4 <- C5 C4 C3 C2 C1 C0 Low bits of BYTEC
9. Write GCR(NIBL1), GCR(NIBL2), GCR(NIBL3) and GCR(NIBL4)

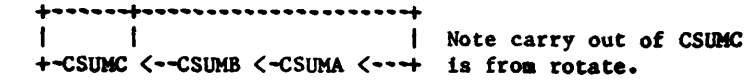


Figure showing carry propagation

apple computer inc.	SIZE A	DRAWING NUMBER 699-0285-A
	SCALE:	SHEET 35 OF 39

GCR Codeword Table (used to convert nibbles to GCR codewords)

0:	96,97,9A,9B,9D,9E,9F,A6
8:	A7,AB,AC,AD,AE,AF,B2,B3
10:	B4,B5,B6,B7,B9,BA,BB,BC
18:	BD,BE,BF,CB,CD,CE,CF,D3
20:	D6,D7,D9,DA,DB,DC,DD,DE
28:	DF,E5,E6,E7,E9,EA,EB,EC
30:	ED,EE,EF,F2,F3,F4,F5,F6
38:	F7,F9,FA,FB,FC,FD,FE,FF

Speed Control

Disk speed is controlled via a PWM signal from the host computer. The duty cycle of this signal is set by software in the host computer; the appropriate value is determined by measuring the length of pulses on the tach sense line from the disk drive. The disk speed should be checked when a diskette is first inserted and periodically thereafter to allow adjustment for thermal drifting of disk speed. The speed should also be checked at the position on the diskette which corresponds to the actual speed group to compensate for torque loading of the motor.

Disk Storage Calculations

The next page shows how the track classes and speeds were determined. The following formulas were used:

track density:	135.4666 tracks/inch
	0.1875 mm track to track
track 0 radius:	39.5 mm
max data density:	8750 fci = 344.4882 fcmm
sync overhead:	6%
bytes/block	733.5
data speed:	500 kbits/sec
bytes:	(733.5 * blocks) * 1.06
rpm:	60 sec/min * 500kbits/sec /(bytes*8bits/byte)
fci:	bytes*8bits/byte/(2*Pi*Radius in inches)

The actual RPM values for Macintosh are adjusted for a bit rate of 489.6 kbits/sec and are slightly lower (e.g., 394 rpm instead of 402 rpm on the outside tracks).

apple computer inc.	SIZE A	DRAWING NUMBER 699-0285-A
	SCALE:	SHEET 36 OF 39

TRACK	RADIUS (side0)	RADIUS (side1)	BLOCKS	BYTES	RPM	FCI (side0)	FCI (side1)
0	39.5	38	12	9330.12	401.9241	7638.955	7940.493
1	39.3125	37.8125	12	9330.12	401.9241	7675.389	7979.867
2	39.125	37.625	12	9330.12	401.9241	7712.172	8019.634
3	38.9375	37.4375	12	9330.12	401.9241	7749.309	8059.799
4	38.75	37.25	12	9330.12	401.9241	7786.806	8100.369
5	38.5625	37.0625	12	9330.12	401.9241	7824.667	8141.349
6	38.375	36.875	12	9330.12	401.9241	7862.899	8182.745
7	38.1875	36.6875	12	9330.12	401.9241	7901.505	8224.565
8	38	36.5	12	9330.12	401.9241	7940.493	8266.815
9	37.8125	36.3125	12	9330.12	401.9241	7979.867	8309.500
10	37.625	36.125	12	9330.12	401.9241	8019.634	8352.629
11	37.4375	35.9375	12	9330.12	401.9241	8059.799	8396.208
12	37.25	35.75	12	9330.12	401.9241	8100.369	8440.244
13	37.0625	35.5625	12	9330.12	401.9241	8141.349	8484.745
14	36.875	35.375	12	9330.12	401.9241	8182.745	8529.717
15	36.6875	35.1875	12	9330.12	401.9241	8224.565	8575.168
16	36.5	35	11	8552.61	438.4626	7577.913	7902.681
17	36.3125	34.8125	11	8552.61	438.4626	7617.042	7945.245
18	36.125	34.625	11	8552.61	438.4626	7656.577	7988.270
19	35.9375	34.4375	11	8552.61	438.4626	7696.524	8031.763
20	35.75	34.25	11	8552.61	438.4626	7736.891	8075.733
21	35.5625	34.0625	11	8552.61	438.4626	7777.683	8120.186
22	35.375	33.875	11	8552.61	438.4626	7818.907	8165.132
23	35.1875	33.6875	11	8552.61	438.4626	7860.571	8210.578
24	35	33.5	11	8552.61	438.4626	7902.681	8256.533
25	34.8125	33.3125	11	8552.61	438.4626	7945.245	8303.005
26	34.625	33.125	11	8552.61	438.4626	7988.270	8350.003
27	34.4375	32.9375	11	8552.61	438.4626	8031.763	8397.536
28	34.25	32.75	11	8552.61	438.4626	8075.733	8445.613
29	34.0625	32.5625	11	8552.61	438.4626	8120.186	8494.245
30	33.875	32.375	11	8552.61	438.4626	8165.132	8543.439
31	33.6875	32.1875	11	8552.61	438.4626	8210.578	8593.207
32	33.5	32	10	7775.1	482.3089	7505.939	7857.780
33	33.3125	31.8125	10	7775.1	482.3089	7548.186	7904.093
34	33.125	31.625	10	7775.1	482.3089	7590.912	7950.955
35	32.9375	31.4375	10	7775.1	482.3089	7634.124	7998.376
36	32.75	31.25	10	7775.1	482.3089	7677.830	8046.366
37	32.5625	31.0625	10	7775.1	482.3089	7722.041	8094.936
38	32.375	30.875	10	7775.1	482.3089	7766.763	8144.095
39	32.1875	30.6875	10	7775.1	482.3089	7812.006	8193.856
40	32	30.5	10	7775.1	482.3089	7857.780	8244.228
41	31.8125	30.3125	10	7775.1	482.3089	7904.093	8295.223
42	31.625	30.125	10	7775.1	482.3089	7950.955	8346.853
43	31.4375	29.9375	10	7775.1	482.3089	7998.376	8399.130
44	31.25	29.75	10	7775.1	482.3089	8046.366	8452.065
45	31.0625	29.5625	10	7775.1	482.3089	8094.936	8505.673
46	30.875	29.375	10	7775.1	482.3089	8144.095	8559.964
47	30.6875	29.1875	10	7775.1	482.3089	8193.856	8614.953

apple computer inc.

SIZE	DRAWING NUMBER
A	699-0285-A
SCALE:	SHEET 37 OF 39

TRACK	RADIUS (side0)	RADIUS (side1)	BLOCKS	BYTES	RPM	FCI (side0)	FCI (side1)
48	30.5	29	9	6997.59	535.8988	7419.805	7803.588
49	30.3125	28.8125	9	6997.59	535.8988	7465.701	7854.371
50	30.125	28.625	9	6997.59	535.8988	7512.168	7905.818
51	29.9375	28.4375	9	6997.59	535.8988	7559.217	7957.945
52	29.75	28.25	9	6997.59	535.8988	7606.859	8010.763
53	29.5625	28.0625	9	6997.59	535.8988	7655.105	8064.287
54	29.375	27.875	9	6997.59	535.8988	7703.968	8118.531
55	29.1875	27.6875	9	6997.59	535.8988	7753.458	8173.510
56	29	27.5	9	6997.59	535.8988	7803.588	8229.238
57	28.8125	27.3125	9	6997.59	535.8988	7854.371	8285.732
58	28.625	27.125	9	6997.59	535.8988	7905.818	8343.006
59	28.4375	26.9375	9	6997.59	535.8988	7957.945	8401.078
60	28.25	26.75	9	6997.59	535.8988	8010.763	8459.965
61	28.0625	26.5625	9	6997.59	535.8988	8064.287	8519.682
62	27.875	26.375	9	6997.59	535.8988	8118.531	8580.248
63	27.6875	26.1875	9	6997.59	535.8988	8173.510	8641.682
64	27.5	26	8	6220.08	602.8861	7314.878	7736.891
65	27.3125	25.8125	8	6220.08	602.8861	7365.095	7793.091
66	27.125	25.625	8	6220.08	602.8861	7416.006	7850.113
67	26.9375	25.4375	8	6220.08	602.8861	7467.625	7907.977
68	26.75	25.25	8	6220.08	602.8861	7519.968	7966.699
69	26.5625	25.0625	8	6220.08	602.8861	7573.051	8026.301
70	26.375	24.875	8	6220.08	602.8861	7626.887	8086.800
71	26.1875	24.6875	8	6220.08	602.8861	7681.495	8148.219
72	26	24.5	8	6220.08	602.8861	7736.891	8210.578
73	25.8125	24.3125	8	6220.08	602.8861	7793.091	8273.898
74	25.625	24.125	8	6220.08	602.8861	7850.113	8338.203
75	25.4375	23.9375	8	6220.08	602.8861	7907.977	8403.516
76	25.25	23.75	8	6220.08	602.8861	7966.699	8469.859
77	25.0625	23.5625	8	6220.08	602.8861	8026.301	8537.259
78	24.875	23.375	8	6220.08	602.8861	8086.800	8605.739
79	24.6875	23.1875	8	6220.08	602.8861	8148.219	8675.328

side 0	blocks	800	max fci side 0	8224.565
side 1	blocks	800	max fci side 1	8675.328
total	blocks	1600	min fci side 0	7314.878
total	bytes	819200	min fci side 1	7736.891

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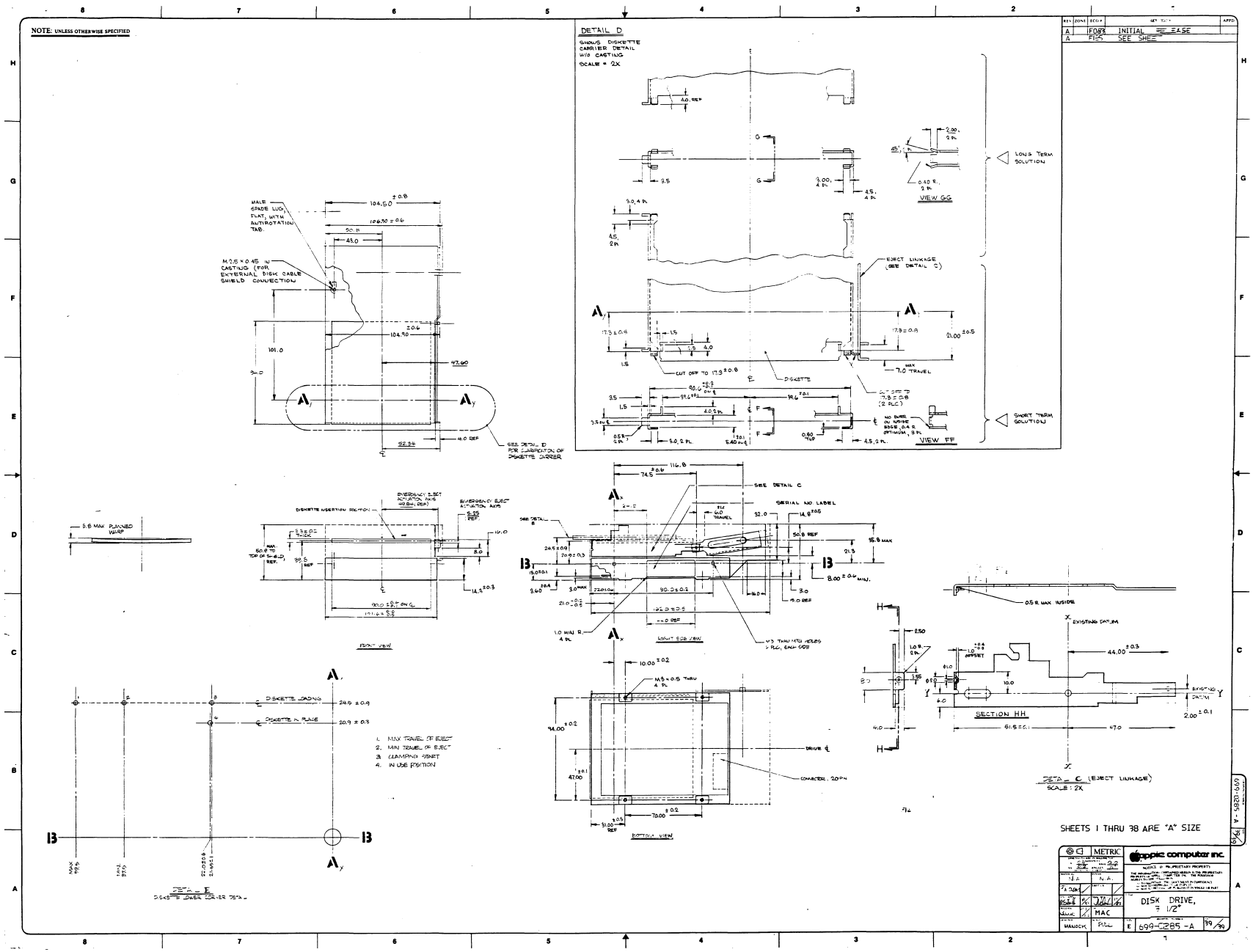
SIZE	DRAWING NUMBER
A	699-0285-A
SCALE:	SHEET 38 OF 39

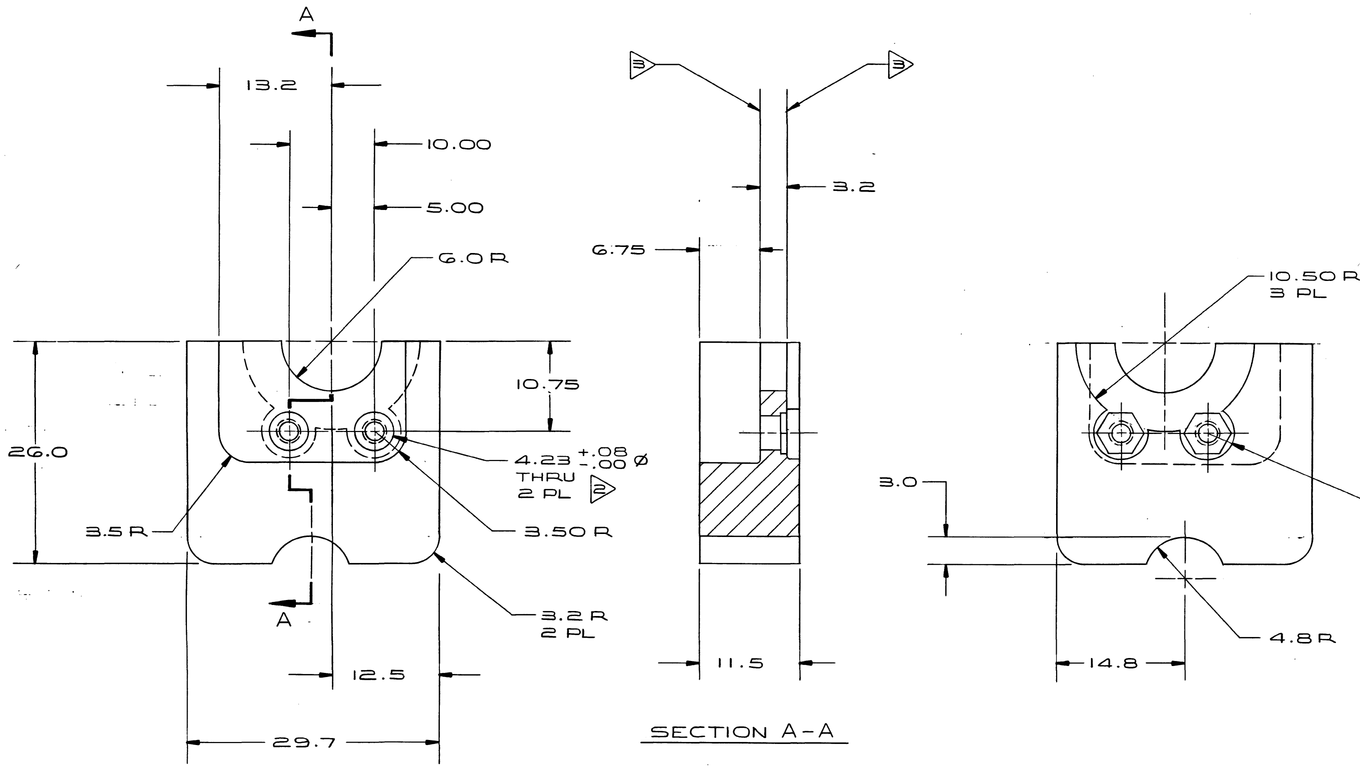


"APPLE_699-0285-A-39of39.PICT" 577 KB 2002-03-12 dpi: 200h x 200v pix: 7747h x 5876v

NOTE: UNLESS OTHERWISE SPECIFIED

1. MATL: LEAD BASE DIE CASTING ALLOY NO.7. 17 % ANTIMONY, 83 % LEAD.
2. DRILL HOLE TO INDICATED SIZE. INSTALL PEM SELF-CLINCHING FLUSH STANDOFF NO. SOS-440-4 (4-40 THD). ORIENTATE AS SHOWN.
3. PEM FASTENERS ARE NOT TO PROTRUDE BEYOND INDICATED SURFACES.
4. UNSPECIFIED RADII TO BE .20 R MAX.
5. COUNTER-WEIGHTS TO BE FREE OF BURRS AND LOOSE OR FOREIGN PARTICLES AND PACKAGED TO PREVENT CONTAMINATION.
6. FINISH: ZINC PLATE PER QQ-Z-325, TYPE 2, CLASS 2.

REV.	ZONE	ECO #	REVISION	APPD
A		PG19	INITIAL RELEASE (SK-W095-08)	



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DRFT: ANDERSON — DESIGNER: ANDERSON — ORIG. DIV: M.S.D. — SCALE: 4X

TITLE: COUNTERWEIGHT, ARM, WIDGET

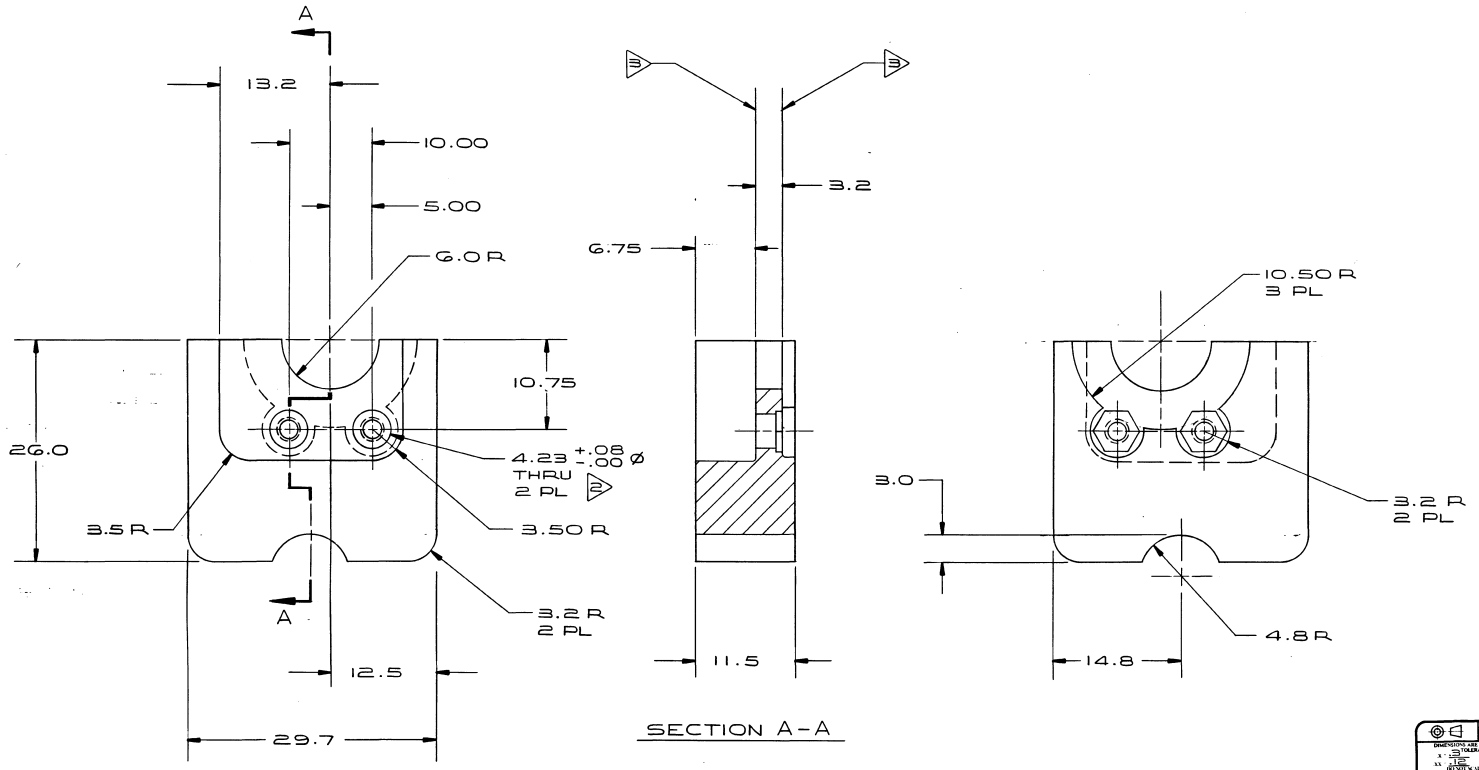
SIZE: D — DRAWING NUMBER: 815-5032-A — SHT 1/1

“APPLE_815-5032-A-1of1.PICT” 546 KB 2002-03-12 dpi: 200h x 200v pix: 8664h x 5618v

REV	ZONE	ECO #	REVISION	APPD
A		P619	INITIAL RELEASE (SK-W095-08)	

NOTE: UNLESS OTHERWISE SPECIFIED

1. MATL : LEAD BASE DIE CASTING ALLOY NO.7. 17 % ANTIMONY, 83 % LEAD.
2. DRILL HOLE TO INDICATED SIZE. INSTALL PEM SELF-CLINCHING FLUSH STANDOFF NO. SOS-440-4 (4-40 THD). ORIENTATE AS SHOWN.
3. PEM FASTENERS ARE NOT TO PROTRUDE BEYOND INDICATED SURFACES.
4. UNSPECIFIED RADII TO BE .20 R MAX.
5. COUNTER-WEIGHTS TO BE FREE OF BURRS AND LOOSE OR FOREIGN PARTICLES AND PACKAGED TO PREVENT CONTAMINATION.
6. FINISH : ZINC PLATE PER QQ-Z-325, TYPE 2, CLASS 2.



METRIC	apple computer inc.	
DRAFT: ANDERSON	TITLE: COUNTERWEIGHT, ARM, WIDGET	
RELEASE	ORIG. DIV.: M.S.D.	
DESIGNER: ANDERSON	SCALE: 4X	SIZE: D — DRAWING NUMBER: 815-5032-A — SHT 1 / 1

815-5032-A 1/1

"APPLE_815-5032-A-1of1b.PICT" 548 KB 2002-03-12 dpi: 200h x 200v pix: 8686h x 5690v