# Sierra Circuit Design, Inc.

## IP_65C02 MICROPROCESSOR CORE

### Key Features:

- 65C02 instruction-set compatible

  70 Instructions, 212 opcodes
  15 addressing modes
  Decimal arithmetic instructions
  Branch-on-bit-set/reset instructions
  Semaphore bit instructions
  Fewer clock cycles per instruction
  64K byte address space

- Small and fast technology-independent design

  In LSI Logic G-10 process:
  90 MHz Fmax (pre-layout)
  .68 mm-square (2-layer metal)
  .48 mm-square (3-layer metal)

  In Altera Flex10K FPGA
  10.2 MHz Fmax (pre-layout)
  930 LCs, (53% of a 10K30)

- Clean-room synthesizable VHDL design
- Fully static synchronous design
- No internal three-state busses
- Easy to modify and add custom instructions
- Easy to use test bench

### Product Description:

MOS Technologies, Inc. first produced the original 6502 processor in 1975. It was later redesigned to fix some design quirks and to add a few instructions. This new design was designated the 65C02. The strengths of the 6502/65C02 architecture are in its small size, flexible-addressing modes and its relatively orthogonal instruction set. These same features make it an excellent choice for an embedded core.

This synthesizable 65C02-compatible core was independently designed from public domain and commercially available data sheets and books. The underlying micro-architecture of the core is different from the original design. This allows many instructions to complete in fewer clock cycles. For example, no instruction in the original design could complete in less than 2 cycles. In contrast, about 10% of the core's instruction set require only a single cycle (all accumulator addressing mode instructions and many implied mode instructions). Many multi-cycle instructions also require fewer cycles. A complete list of opcode timings is available as part of the documentation package.

Two interrupt lines are provided IRQ (maskable) and NMI (non-maskable). Interrupts are serviced after the currently executing instruction is complete. Since the longest instruction is 5 cycles long, and the IRQ takes another 5 cycles to save the current PC and flags and to load the PC with the interrupt vector, the maximum interrupt latency is 10 clock cycles.

A ready line is provided for interfacing with slow memory or peripherals. It also allows the user to single-step the core. RDY is sampled on the falling edge of the PHI2 input clock. If RDY is sampled low, the processor will hold its current state until RDY is sampled high.

Only a single clock (PHI2) is required. All state transitions occur on the falling edge of this clock, so precise clock symmetry is not required. Your exact system clock rate will depend on your synthesis tools and memory access time, but in a modern CMOS process technology, system clock rates of 50 to 100 MHz should be easily achievable.

The core was tested for 65C02 compatibility by using both a simulation test suite and an FPGA validation board. The validation board adapts an Altera 10K30 FPGA into the 65C02 40-pin-DIP footprint. This board was then plugged into an Apple IIe. Several versions of Apple DOS were booted and many application programs were run successfully.