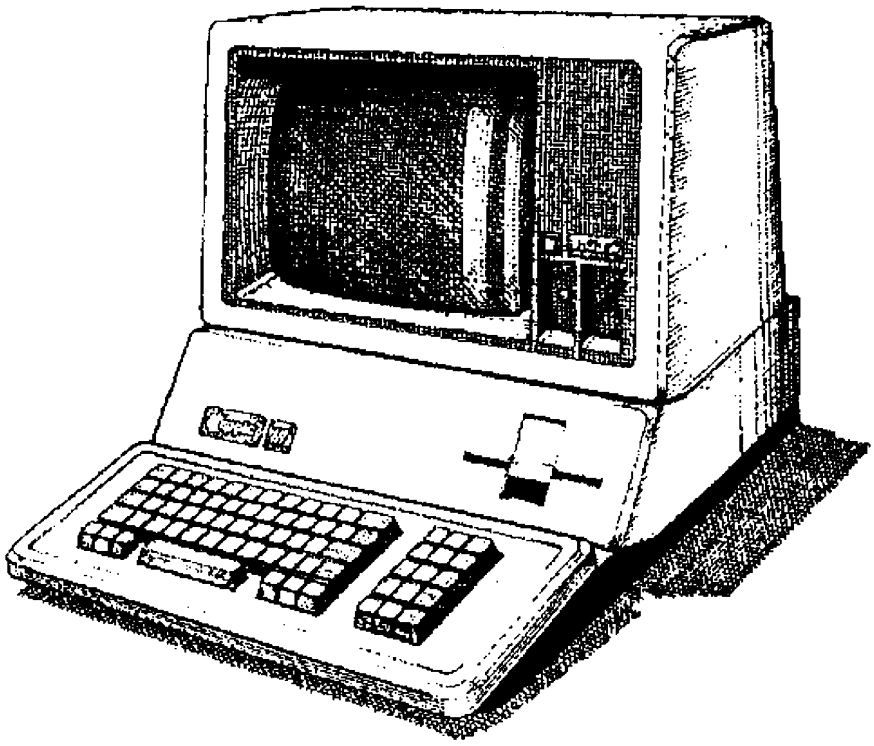
Apple /// Computer Information

# Apple /// Service Reference Manual



## Section I of II • Theory of Operation

## Chapter 3 • The Versatile Interface Adapter (VIA)

Written by Apple Computer • 1982

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# THE VERSATILE INTERFACE ADAPTER

## GENERAL

The Versatile Interface Adapter (VIA), as used in the Apple ///, is a very flexible I/O control device which minimizes the discrete control circuitry on the Main Logic Board. There are two VIAs used in the system.

Each VIA contains two 8-bit I/O ports, a serial port, and two 16-bit interval timers, as shown in the VIA Block Diagram. Each of the sections is very flexible and can be utilized in many operating modes. In the Apple ///, however,some of these modes cannot be used because of certain hardware design considerations.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves, or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register, and a pair of function control registers are provided.

Before we get into a functional description of how the VIA is used in the Apple ///, let's first go through a pin description of the it.

## VIA [6522] PIN DESCRIPTIONS

RES* (Reset) (34)

The Reset input clears all internal registers to logic 0 (except T1 and T2 latches and counters, and the shift register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc., and disables interrupting from the chip. On both VIAs this pin (34) is connected to the RESET* of the system. The system generates the reset at power on, or at depression of the Reset switch in conjunction with the Control key. (Note the latter may be disabled.)

O2 (Input Clock) (25)

The Input Clock is the system PRE1M (PRE-1 MHZ) clock which operates at 1MHZ and is used to trigger all data transfers between the system processor and the VIA. The PRE1M, developed in the system timing circuits, is used within the device to clock the various functions of the registers and timers.

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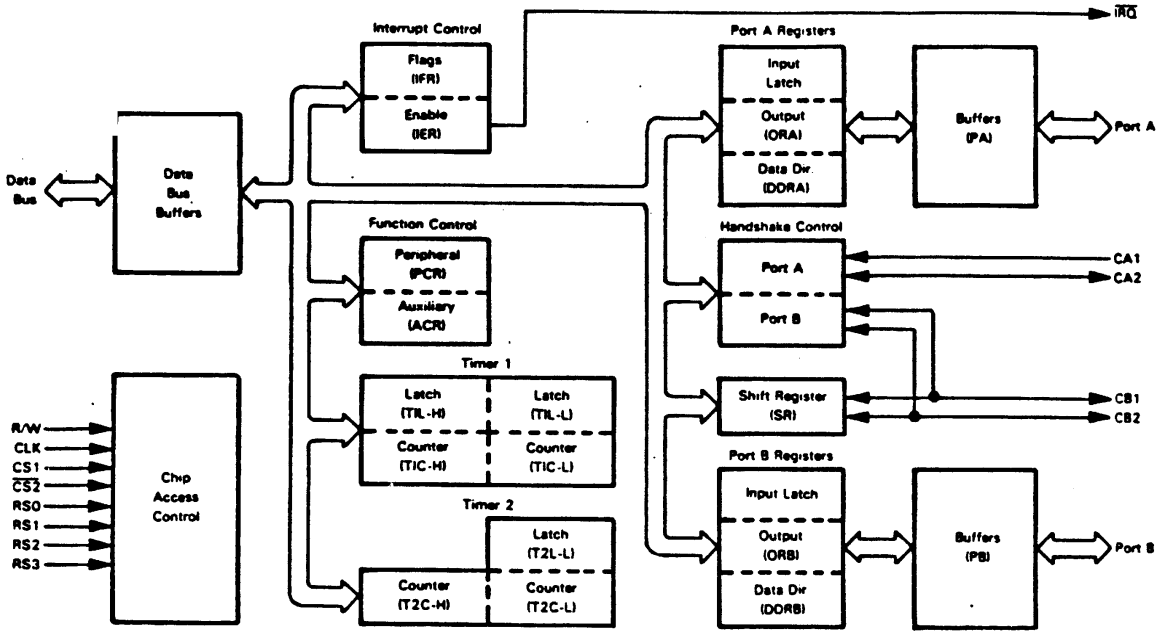


Block Diagram of the 6522 Versatile Interface Adapter

Addressing 6522 VIA Internal Registers

| Label | Select Lines | | | | Addressed Location |
|---|---|---|---|---|---|
| | RS3 | RS2 | RS1 | RS0 | |
| DEV | 0 | 0 | 0 | 0 | Output register for I/O Port B |
| DEV+1 | 0 | 0 | 0 | 1 | Output register for I/O Port A, with handshaking |
| DEV+2 | 0 | 0 | 1 | 0 | I/O Port B Data Direction register |
| DEV+3 | 0 | 0 | 1 | 1 | I/O Port A Data Direction register |
| DEV+4 | 0 | 1 | 0 | 0 | Read Timer 1 Counter low-order byte<br>Write to Timer 1 Latch low-order byte |
| DEV+5 | 0 | 1 | 0 | 1 | Read Timer 1 Counter high-order byte<br>Write to Timer 1 Latch high-order byte and initiate count |
| DEV+6 | 0 | 1 | 1 | 0 | Access Timer 1 Latch low-order byte |
| DEV+7 | 0 | 1 | 1 | 1 | Access Timer 1 Latch high-order byte |
| DEV+8 | 1 | 0 | 0 | 0 | Read low-order byte of Timer 2 and reset Counter interrupt<br>Write to low-order byte of Timer 2 but do not reset interrupt |
| DEV+9 | 1 | 0 | 0 | 1 | Access high-order byte of Timer 2, reset Counter interrupt on write |
| DEV+A | 1 | 0 | 1 | 0 | Serial I/O Shift register |
| DEV+B | 1 | 0 | 1 | 1 | Auxiliary Control register |
| DEV+C | 1 | 1 | 0 | 0 | Peripheral Control register |
| DEV+D | 1 | 1 | 0 | 1 | Interrupt Flag register |
| DEV+E | 1 | 1 | 1 | 0 | Interrupt Enable register |
| DEV+F | 1 | 1 | 1 | 1 | Output register for I/O Port A, without handshaking |

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R/W* (Read/Write) (22)

The direction of the data transfers between the 6522 and the system processor is controlled by the R/W* line, which is driven by the Internal Read/Write, I R/W*, signal generated by the processor.

If pin 22 is low, data will be transferred out of the processor into the selected VIA register, as in a write operation.

If R/W is high, data will be transferred out of the selected 6522 register, as in a read operation.

DB0-DB7 (Data Bus) (33-26)

The eight bi-directional data bus lines (in the Internal Data Bus) are used to transfer data between the VIA and the system processor.

- During read cycles, the contents of the selected register are placed on the data bus lines and transferred into the processor.
- During the write operation, these lines are high-impedance inputs and data is transferred from the processor into the selected register.
- When the 6522 is unselected, the data bus lines are at high-impedance. These lines are connected to the Internal Data Bus and are not accessable from the outside world.

CS1, CS2* (Chip Selects) (24,23)

These two chip select lines are connected to direct decodes of the processor's address bus.

- CS1 on both VIAs is controlled by the signal CS6522, a signal which is qualified by other system consideration.
- CS2 is driven by the signal FFDX for IC at location B5, and FFEX for IC9 at location B6. The selected VIA register will be accessed when CS1 is high and CS2 is low.

RS0-RS3 (Register Selects) (38-35)

The four Register Select inputs permit the system processor to select one of the 16 internal registers, each of which performs a specific function, of the VIA as shown in the accompanying table.

IRQ (Interrupt Request) (21)

The Interrupt Request output goes low whenever an internal (to the VIA) flag is set and the corresponding interrupt enable bit is at 1. This output is

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open-drain" to allow the interrupt request signal to be "wired-OR'ED" with other equivalent signals in the system.

PA0-PA7 (Peripheral A Port) (2-10)

The PA port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a data direction register.

The output is controlled by an output register. Input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers.

On standard TTL load, these lines are present in the input mode. Conversely, on standard TTL load, they will drive in the output mode.

CA1, CA2 (Peripheral A Control Lines) (40,39)

The two PA control lines can act as interrupt inputs (as used in the Apple ///) or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit.

PB0-PB7 (Peripheral B Port) (11-17)

The PB port consists of 8 bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port.

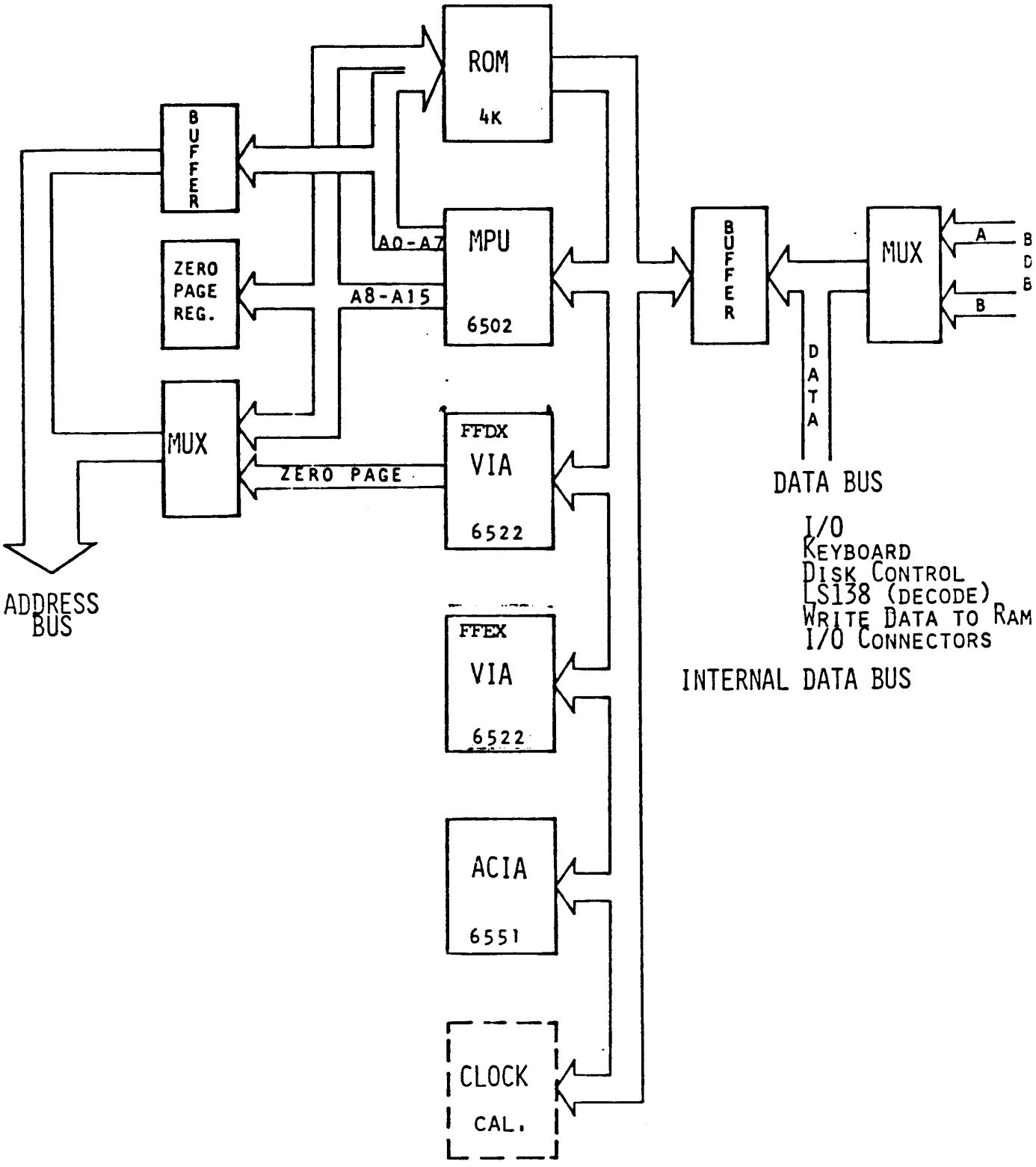
The polarity of the PB7 output signal can be controlled by one of the interval timers, while the second timer can be programmed to count pulses on the PB6 pin.

Peripheral B lines represent one TTL load in the input mode and drive one standard load in the output mode.

CB1, CB2 (Peripheral B Control Lines) (18-19)

The PB control lines act as interrupt inputs or as handshake outputs. As with the CA lines, each line controls an interrupt flag.

These lines also act as a serial port under control of the Shift Register. They have loading and driving characteristics identical to the CA control lines.


ROM
4K
BUFFER
MPU
6502
A0-A7
A8-A15
ZERO PAGE REG.
MUX
ZERO PAGE
FFDX
VIA
6522
FFEX
VIA
6522
ACIA
6551
CLOCK
CAL.
ADDRESS BUS
BUFFER
MUX
A
B
D
B
DATA
DATA BUS
I/O
KEYBOARD
DISK CONTROL
LS138 (DECODE)
WRITE DATA TO RAM
I/O CONNECTORS
INTERNAL DATA BUS

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## VIA FUNCTIONAL DESCRIPTION

### Port A and Port B Operation

Each 8-bit peripheral port has a Data Direction Register for specifying whether the Peripheral pins are to act as inputs or outputs.

- o A "0" in a bit of the DDR causes the corresponding peripheral pin to act as an input.
- o A "1" causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register and a bit in the Input Register. When the pin is programmed as an output, the voltage on the pin is controlled by the corresponding bit of the output Register. A one in the ORX causes the output to go high; a zero causes the output to go low.

Data may be written into ORX bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

The IRB Register operation is similar to that of the IRA. For pins programmed as outputs, however, there is a difference. When reading the IRB, it is the bit stored in the ORB that is sensed. That means the buffering and gating on the two ports differ in respect to pins programmed as outputs.

See the figures below detailing the data bytes programmed into the DDRs and the two control registers for each of the VIAs. Compare these with the environments of each device.

### Timer Operation

Interval Timer T1 consists of two 8-bit latches and a 16 bit counter. The latches are used to store data which is to be loaded into the counter. After loading, the counter decrements at the rate of PRE1M.

Upon reaching zero, an interrupt flag will be set; if the interrupt is enabled, the IRQ* will go low. The timer will then disable any further interrupts, or will automatically transfer the contents of the latches into the counter and will continue to decrement.

In addition, the timer may be programmed to invert the output signal on a peripheral pin each tme it "times out." Each of these modes is discussed below.

### Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each timer load operation. As with any interval timer, the delay between the write T1C-H (FFD5, FFE5) operation and generation of the processor interrupt

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is a di... function of the data loaded into the timer.

In the one-shot mode, writing into the high order latch has no effect on the operation of Timer 1. However, it is necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation.

When the processor writes into the high order counter

- o the T1 interrupt flag is cleared;
- o the contents of the low order latch are transferred into the low order counter;
- o the timer again begins to decrement at the PRE1M rate.

After the timer reaches its time out, it continues to decrement until it is reset with the proper write operation.

The processor may read the current count of the timer to determine how long it has been since the interrupt has been set. Reading the counter does not reset the interrupt flag or the timer.

### Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts. These interrupts are accomplished in the "free-running mode."

In the free-running mode, the interrupt flag is set each time the counter reaches zero. However, instead of continuing to decrement from zero, the timer automatically reloads the contents of the high and low latches, and continues to decrement from there. In this mode, the interrupt flag can be cleared by writing T1C-H, or reading T1C-L, or by writing directly to the interrupt flag.

It is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out. All of the interval timers are "retriggerable." Rewriting the counter will always re-initialize the time-out period.

### Timer 2 Operation

Timer 2 operates as an interval timer in the one-shot mode only, or as a counter of negative pulses on the PB6 peripheral pin. A single bit in the ACR is provided for this mode selection.

Timer 2 is comprised of a write-only low order latch, a read-only low order counter, and a read/write high order counter.

### Timer 2 One Shot-Mode

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As an interval timer, T2 operates very much like T1 in the one-shot mode. Setting of the interrupt flag, however, will be disabled after the first time out, and it will not be set again until the write T2C-H operation.

The flag can be reset by reading T2C-L, or by writing T2C-H.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on the P6 pin. This is accomplished by first loading a number into T2, which clears the interrupt flag and allows the counter to be decremented by the pulses on PB6. The interrupt flag will be set when T2 is decremented to zero. The counter will continue to decrement.

Note that it is necessary to rewrite the timer to re-enable the subsequent interrupt flags.

Shift Register Operation

The Shift Register performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which set the various register modes are located in the ACR. In total, there are eight modes for this register. The primary use of the shift register is control of the serial printer port.

In the FFEX VIA, the shift register can be activated to "count" 8 VBL (Vertical Blanking) pulses. The shift register sets its interrupt flag each time it completes 8 shifts.

Refer to the figure below for descriptions of the various modes of the shift register.

Interrupt Operation

Controlling interrupts within the VIA involves three principal operations. These are:

- o flagging the interrupts
- o enabling the interrupts
- o signalling the processor that an interrupt condition has occurred.

Interrupt flags are set by interrupting conditions which exist within the chip, or on inputs to the chip. These flags normally remain set until the

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interrupt has been serviced by the processor. To determine the source of an interrupt, the processor must examine these flags in order from highest to lowest priority.

Procedure:

1. Read the flag register into the accumulator.

2. Shift it right or left.

3. Use conditional branch instructions to detect an active interrupt.

Associated with each flag bit is an enable bit. This can be set or cleared by the processor to enable or disable the flag respectively. If a flag bit is enabled and set, it will cause the IRQ* output to go low, thus sending a direct request to the processor. In addition, bit 7 of the flag register is set to allow quick determination of which chip contains an interrupt condition.

The IFR may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register controls are applied to the chip, the contents of the IFR are placed on the Data Bus. Bit 7 indicates the condition of the IRQ output, however it cannot be directly cleared; all other bits must be cleared in order for this bit to become inactive.

For each interrupt flag in the IFR there is a corresponding bit in the Interrupt Enable Register. This is accomplished by writing to the IER. There are two steps to consider: the enabling write cycle and the disabling write cycle. The cycle is determined by the logic state of bit 7:

- If bit 7 and the corresponding 0-6 bits are at "1", the 0-6 bits enable their matching flag.

- If bit 7 is a 0, then the 0-6 bits containing a "1" disable the matching flag.

Refer to the figures to see the data byte configuration and device.

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## 6522 VIA Environment and Control

The description so far has been very general and has not completely detailed the functions of the two VIAs within the Apple ///. However, one must be familiar with the many registers and modes to understand how the VIA is utilized and how it can be configured for various operations.

The following figures and tables detail the environment and address locations of each of the registers and I/O pins for the two chips. (Many of the signals are common controls or busses; their descriptions relate to both devices.)

### ID0-ID7

The data bus pins of the VIA are connected to the associated pins of the Internal Data bus. When the chip is properly addressed and selected, each of the various registers may be accessed for reading or writing data, control bytes, status or timer states. It is this bus through which all data passes to the system and/or processor.

### Reset

The RES pin is connected to the RESET line. The system generates the reset at Power On or when the Reset switch is depressed with the Control key.

(Note: the Control key may be software disabled.)

### I R/W*

The R/W* pin is connected directly to the processor's internal Read/Write line. This signal cannot be accessed from the outside world. It is obviously used to control the direction of the data to or from the device.

### PRE1M

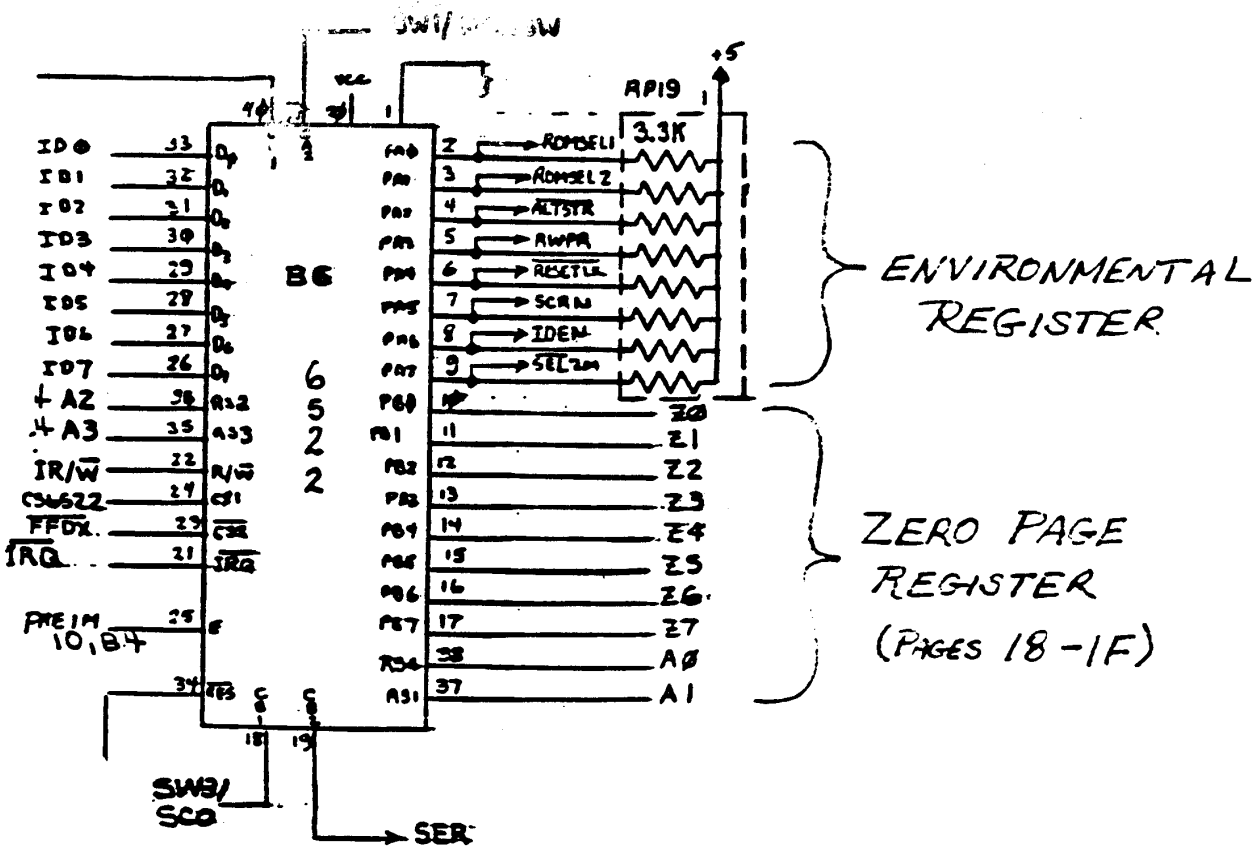
The 02 clock pin is driven by the PRE1M signal developed in the system timing circuits. It is used within the device to clock the various functions of the registers and timers.

### CS6522

This signal is developed under Rom decode of various address states or ranges and other mode selections, and drives the CS1 line of both VIAs.

### A0-A3

The processor's address lines directly drive the Register Select input lines.




| ADDRESS | Register Number | RS Coding | | | | Register Desig. | Description | |
|---|---|---|---|---|---|---|---|---|
| | | RS3 | RS2 | RS1 | RS0 | | Write | Read |
| FFD0 | 0 | 0 | 0 | 0 | 0 | ORB/IRB | Output Register "B" | Input Register "B" |
| FFD1 | 1 | 0 | 0 | 0 | 1 | ORA/IRA | Output Register "A" | Input Register "A" |
| FFD2 | 2 | 0 | 0 | 1 | 0 | DDRB | Data Direction Register "B" | |
| FFD3 | 3 | 0 | 0 | 1 | 1 | DDRA | Data Direction Register "A" | |
| FFD4 | 4 | 0 | 1 | 0 | 0 | T1C-L | T1 Low-Order Latches | T1 Low-Order Counter |
| FFD5 | 5 | 0 | 1 | 0 | 1 | T1C-H | T1 High-Order Counter | |
| FFD6 | 6 | 0 | 1 | 1 | 0 | T1L-L | T1 Low-Order Latches | |
| FFD7 | 7 | 0 | 1 | 1 | 1 | T1L-H | T1 High-Order Latches | |
| FFD8 | 8 | 1 | 0 | 0 | 0 | T2C-L | T2 Low-Order Latches | T2 Low-Order Counter |
| FFD9 | 9 | 1 | 0 | 0 | 1 | T2C-H | T2 High-Order Counter | |
| FFDA | A 10 | 1 | 0 | 1 | 0 | SR | Shift Register | |
| FFDB | B 11 | 1 | 0 | 1 | 1 | ACR | Auxiliary Control Register | |
| FFDC | C 12 | 1 | 1 | 0 | 0 | PCR | Peripheral Control Register | |
| FFDD | D 13 | 1 | 1 | 0 | 1 | IFR | Interrupt Flag Register | |
| FFDE | E 14 | 1 | 1 | 1 | 0 | IER | Interrupt Enable Register | |
| FFDF | F 15 | 1 | 1 | 1 | 1 | ORA/IRA | Same as Reg 1 Except No "Handshake" | |

SY6522 Internal Register Summary

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These four addresses, along with the two chip select lines, activate the chip for access to and from the data bus. You can see that the decimal equivalent of the address (Register Select) lines equals the register number, as detailed in the port address tables.

To determine the complete I/O location:

- Express the A0-A7 bits in Hex
- Substitute the Hex expression for the "x" in the signal name applied to the CS2 input.

IRQ*

The Interrupt Request line is a wire OR'ED bus, shared with the other LSI devices within the system which directly interrupt the processor. The VIA can generate an interrupt due to internal status and can be configured to interrupt on various input conditions. Each VIA provides indirect interrupts to the processor for the other devices in the system, including the slot interrupts. By polling the VIAs, the processor can quickly determine which device or group of devices needs servicing.

VIA (FFDX)

This VIA has the following responsibilities:

- Environmental Register
- Zero Page Register
- Global Interrupt Request
- Serial Data Port Interrupt & Clocking (Silentype)

The signals of the IC at location B6 which are not common to both 6522s are either the port I/Os or the chip select line, CS2.

FFDX

This signal comes from the Device Select logic, and is true for the 16 address states, FFD0 through FFDF.

The table below shows how the signal FFDX (CS2) and the Address Lines on the Register Select Inputs access each of the 16 registers within the VIA.

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Port A Description

The ORA for this device is also called the "Environmental Register" by the system. It is programmed to all outputs, and contains various control mode states which may be software modified.

PA0 and PA1 are used as software switches to control which set of Roms are to be used by the system, and also to indicate there is an expanded set of Rom in the system.

PA2 provides the software switch that enables the Apple /// to switch between two memory stacks.

PA3 is a software switch which will enable or disable the system for writing into the Ram. It can be set for entire banks or it can be set at will to disallow writing into memory.

PA4 is a software switch which will cause the function of the Reset switch to be ignored, and will simultaneously disable the Non-Maskable Interrupts from the I/O slots.

PA5 contains the switch "Scrn" (Screen) which is used to modify the Blanking signal.

Global IRQ

The CA1 line is connected to "OR" function of the slot IRQs. If any slot is requesting an interrupt, this line will toggle. The VIA then generates an IRQ and sets the associated Interrupt flag.

Swl/Mgnsw

This line connected to the CA2 line can be programmed to cause an interrupt on either edge of transition. It could be used to have a Function Only run while the switch is depressed, or vice versa.

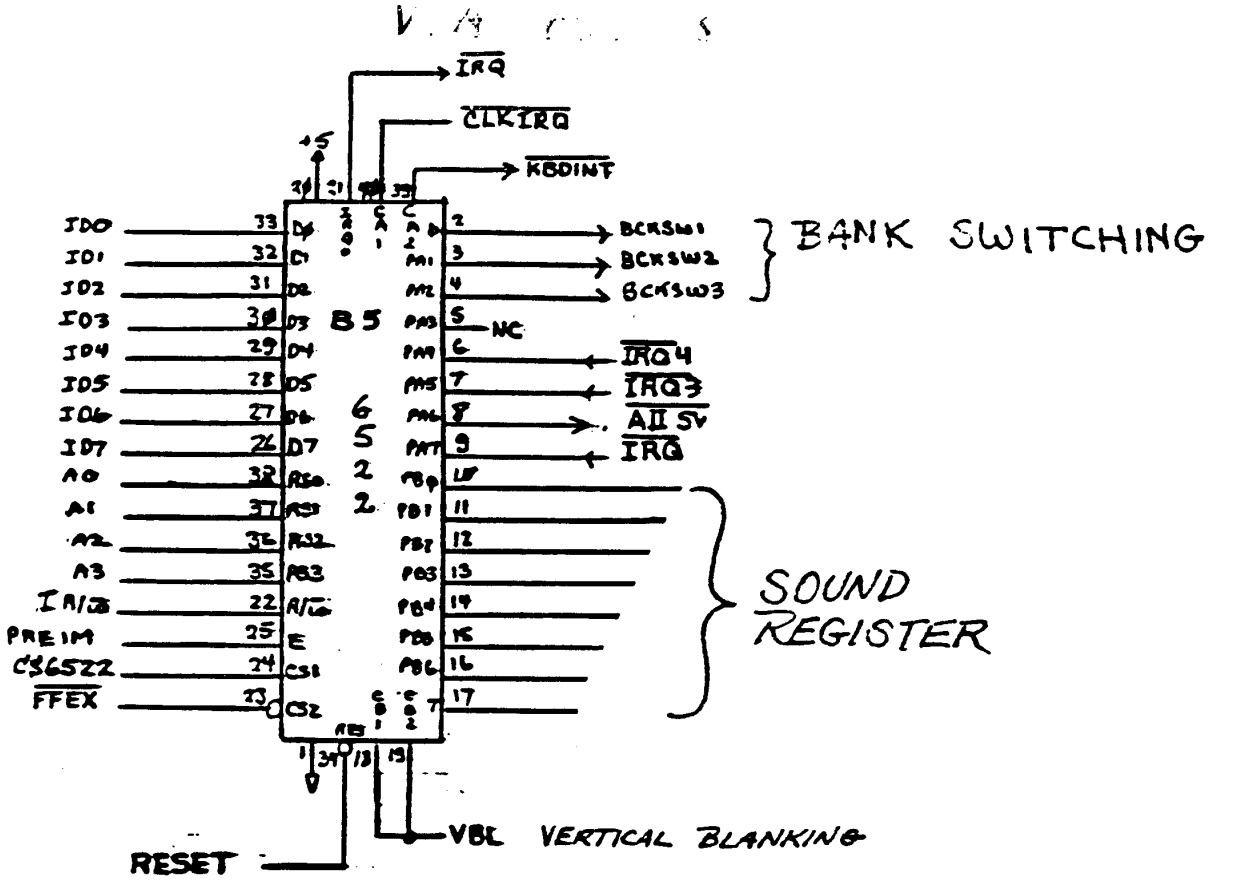
SCO/SER

These two signals form a very elementary serial data port. They are usually programmed as data, and strobe to a serial RO printer.

The port may also be configured as a serial input register or simply as interrupts for the two external lines.

SCO/SER are connected to CB1 and CB2 respectively.

Z0-Z7 (Zero Page Register)




| ADDRESS | Register Number | RS Coding | | | | Register Desig. | Description | |
|---|---|---|---|---|---|---|---|---|
| | | RS3 | RS2 | RS1 | RS0 | | Write | Read |
| FFE0 | 0 | 0 | 0 | 0 | 0 | ORB/IRB | Output Register "B" | Input Register "B" |
| FFE1 | 1 | 0 | 0 | 0 | 1 | ORA/IRA | Output Register "A" | Input Register "A" |
| FFE2 | 2 | 0 | 0 | 1 | 0 | DDRB | Data Direction Register "B" | |
| FFE3 | 3 | 0 | 0 | 1 | 1 | DDRA | Data Direction Register "A" | |
| FFE4 | 4 | 0 | 1 | 0 | 0 | T1C-L | T1 Low-Order Latches | T1 Low-Order Counter |
| FFE5 | 5 | 0 | 1 | 0 | 1 | T1C-H | T1 High-Order Counter | |
| FFE6 | 6 | 0 | 1 | 1 | 0 | T1L-L | T1 Low-Order Latches | |
| FFE7 | 7 | 0 | 1 | 1 | 1 | T1L-H | T1 High-Order Latches | |
| FFE8 | 8 | 1 | 0 | 0 | 0 | T2C-L | T2 Low-Order Latches | T2 Low-Order Counter |
| FFE9 | 9 | 1 | 0 | 0 | 1 | T2C-H | T2 High-Order Counter | |
| FFEA | 10 | 1 | 0 | 1 | 0 | SR | Shift Register | |
| FFEB | 11 | 1 | 0 | 1 | 1 | ACR | Auxiliary Control Register | |
| FFEC | 12 | 1 | 1 | 0 | 0 | PCR | Peripheral Control Register | |
| FFED | 13 | 1 | 1 | 0 | 1 | IFR | Interrupt Flag Register | |
| FFEE | 14 | 1 | 1 | 1 | 0 | IER | Interrupt Enable Register | |
| FFEF | 15 | 1 | 1 | 1 | 1 | ORA/IRA | Same as Reg 1 Except No "Handshake" | |

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The PB port is referred to as the Zero Page Register. In other words, its primary function is to store the current "Zero Page" of the memory. The Apple /// is capable of moving the Zero Page, a feature which greatly enhances the flexibility of the system.

The PB port has a secondary function; it also serves as the address register for the Real Time Clock. The RTC must have the addresses stable for an extended period of time, so instead of adding another latch in the hardware, the designers use this port for control.

Note that each time the port is used for the RTC function it must be restored to the current Zero Page setting.

VIA (FFEX)

This VIA aids in providing the following:

- o Bank Switching
- o Sound Register
- o Interrupt Recognition-clock, keyboard

The signals connected to the VIA located at B5 which are not common to both VIAs are:

- o the A and B port I/Os,
- o the port control lines, and
- o the CS2 line.

FFEX

This signal corresponds to FFDX in that it is true for a group of 16 addresses. See the corresponding table for the complete detail of the register access locations.

Port A Description

The PA0-PA2 lines are configured as outputs and contain the software switches for the Ram banks. Currently, the system segregates the 128K memory into three banks. The decimal decode of the binary bit weight reveals the bank.

The PA4-PA7 lines are configured as inputs. Slot 1 and 2 IRQs, the Solid Apple switch, and the IRQ line itself form the respective inputs.

If it's interrupted, the processor will poll the VIAs first to get a quick look at most of the system. It can then identify and service the requesting device faster, since it doesn't need to poll each individual device.

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The processor can, at certain times, read this port for the status of the special Apple switch on the keyboard without disturbing the keyboard circuit.

The IRQ* signal is wrapped around to the PA7 line for special diagnostic purposes.

CLK IRQ*

The Real Time Clock's interrupt is connected to the CA1 line, which is programmed to be a negative edge active input. When the clock generates an interrupt, it will set the IRA flag in the IFR. The PA port is conditioned for non-latching, however, resulting in a basically independent interrupt for the clock.

Keyboard Interrupt

The keyboard's interrupt is connected to the CA2 input, which is programmed to be an independent negative edge interrupt. It will set Bit 0 in the IFR and cause the IRQ* line to go low.

Note: The keyboard can, for the most part, be disabled by disabling the interrupt flag for the CA2 line.

VBL (Vertical Blanking)

This input can perform two functions, depending on how the CB1, CB2, and Shift Register are programmed.

- The system may want to be interrupted at each vertical blanking cycle. If so, you would program the CB2 line to be an independent interrupt OR let it strobe the IPB and set the corresponding bit flag.
- The system may want to synchronize an operation to the display, but may not want to be interrupted at each VBL. If this is the case, the system can configure the Shift Register to count 8 occurrences of the VBL signal. An interrupt will then occur after each set of 8 Vertical Blanking cycles (about once every second), in sync with the display scan.

PB Port Description

The first 6 lines of the B port are configured to be outputs. They are inputs to the sound Generator.

- The tone generated at the speaker can be varied by changing the bit values of these lines.
- There are 127 possible tone combinations; the missing one turns the tone off completely.

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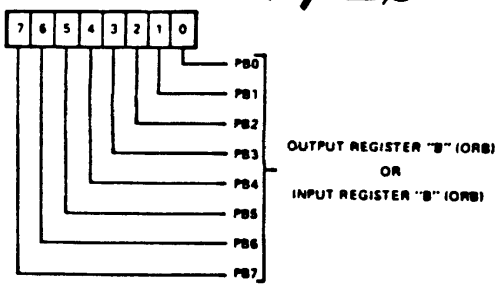
PB6 is connected to the I/O Count line. Depending on the device in the slots, the VIA may be programmed to count a certain number of pulses generated or to determine that only one pulse occurred. Either way, the VIA will generate an IRQ and set the appropriate bit flag.

The last bit is used to monitor the NMI (Non Maskable Interrupt) line generated by the devices in the I/O slots.

VIA APPENDICES

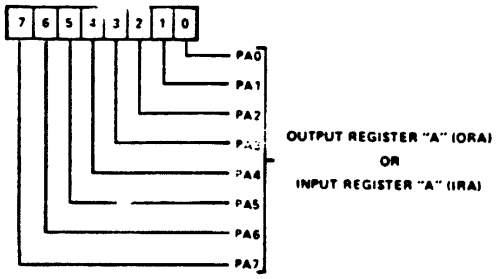
REG 0 – ORB/IRB FFD0/E0




| Pin Data Direction Selection | WRITE | READ |
|---|---|---|
| DDRB = "1" (OUTPUT) | MPU writes Output Level (ORB) | MPU reads output register bit in ORB. Pin level has no affect. |
| DDRB = "0" (INPUT) (Input latching disabled) | MPU writes into ORB, but no effect on pin level, until DDRB changed. | MPU reads input level on PB pin. |
| DDRB = "0" (INPUT) (Input latching enabled) | | MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition. |

Figure 9. Output Register B (ORB), Input Register B (IRB)

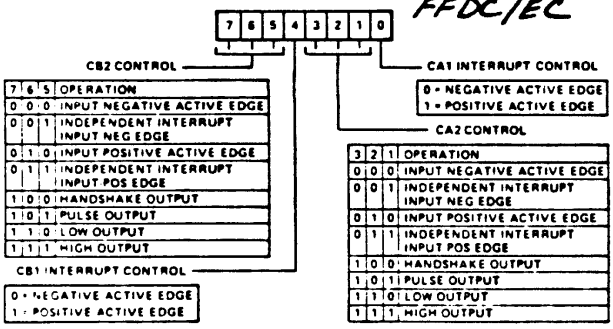
REG 1 – ORA/IRA FFE1/D1




| Pin Data Direction Selection | WRITE | READ |
|---|---|---|
| DDRA = "1" (OUTPUT) (Input latching disabled) | MPU writes Output Level (ORA) | MPU reads level on PA pin. |
| DDRA = "1" (OUTPUT) (Input latching enabled) | | MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition |
| DDRA = "0" (INPUT) (Input latching disabled) | MPU writes into ORA, but no effect on pin level, until DDRA changed | MPU reads level on PA pin. |
| DDRA = "0" (INPUT) (Input latching enabled) | | MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition. |

Figure 10. Output Register A (ORA), Input Register A (IRA)

REG 12 – PERIPHERAL CONTROL REGISTER FFDC/EC

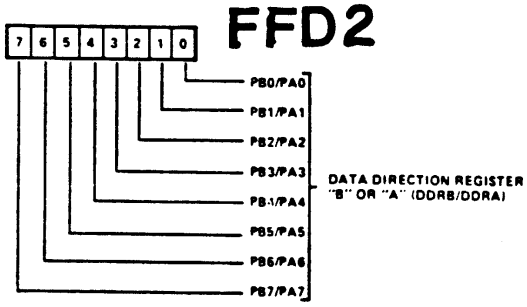



| 7 6 5 | OPERATION |
|---|---|
| 0 0 0 | INPUT NEGATIVE ACTIVE EDGE |
| 0 0 1 | INDEPENDENT INTERRUPT INPUT NEG EDGE |
| 0 1 0 | INPUT POSITIVE ACTIVE EDGE |
| 0 1 1 | INDEPENDENT INTERRUPT INPUT POS EDGE |
| 1 0 0 | HANDSHAKE OUTPUT |
| 1 0 1 | PULSE OUTPUT |
| 1 1 0 | LOW OUTPUT |
| 1 1 1 | HIGH OUTPUT |

| 3 2 1 | OPERATION |
|---|---|
| 0 0 0 | INPUT NEGATIVE ACTIVE EDGE |
| 0 0 1 | INDEPENDENT INTERRUPT INPUT NEG EDGE |
| 0 1 0 | INPUT POSITIVE ACTIVE EDGE |
| 0 1 1 | INDEPENDENT INTERRUPT INPUT POS EDGE |
| 1 0 0 | HANDSHAKE OUTPUT |
| 1 0 1 | PULSE OUTPUT |
| 1 1 0 | LOW OUTPUT |
| 1 1 1 | HIGH OUTPUT |

Figure 14. CA1, CA2, CB1, CB2 Control

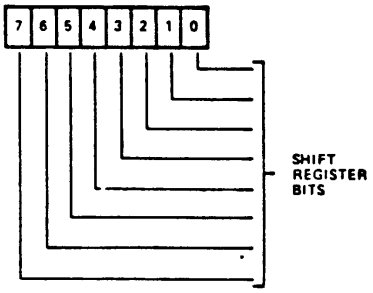
REG 2 (DDRB) AND REG 3 (DDRA) FFD2




"0" ASSOCIATED PB/PA PIN IS AN INPUT (HIGH IMPEDANCE)

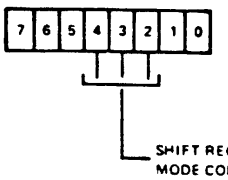
"1" ASSOCIATED PB/PA PIN IS AN OUTPUT, WHOSE LEVEL IS DETERMINED BY ORB/ORA REGISTER BIT.

REG 10 – SHIFT REGISTER FFEA/DA




NOTES:
1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.

REG 11 – AUXILIARY CONTROL REGISTER FFDB/EB




| 4 3 2 | OPERATION |
|---|---|
| 0 0 0 | DISABLED |
| 0 0 1 | SHIFT IN UNDER CONTROL OF T2 |
| 0 1 0 | SHIFT IN UNDER CONTROL OF Φ2 |
| 0 1 1 | SHIFT IN UNDER CONTROL OF EXT CLK |
| 1 0 0 | SHIFT OUT FREE RUNNING AT T2 RATE |
| 1 0 1 | SHIFT OUT UNDER CONTROL OF T2 |
| 1 1 0 | SHIFT OUT UNDER CONTROL OF Φ2 |
| 1 1 1 | SHIFT OUT UNDER CONTROL OF EXT CLK |

Figure 22. SR and ACR Control Bits

Two bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of the T1 operating modes. The four possible modes are depicted in Figure 17.

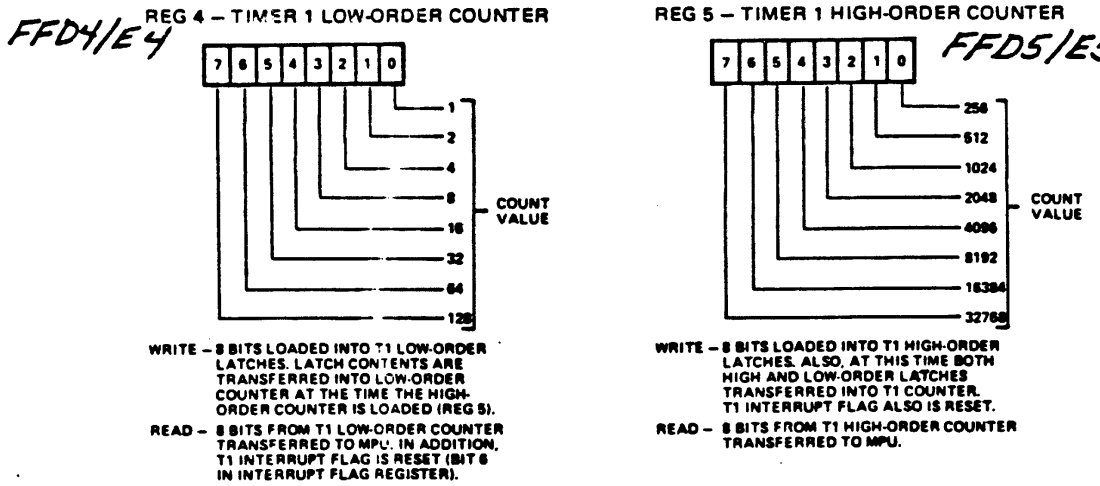



**Figure 15. T1 Counter Registers**

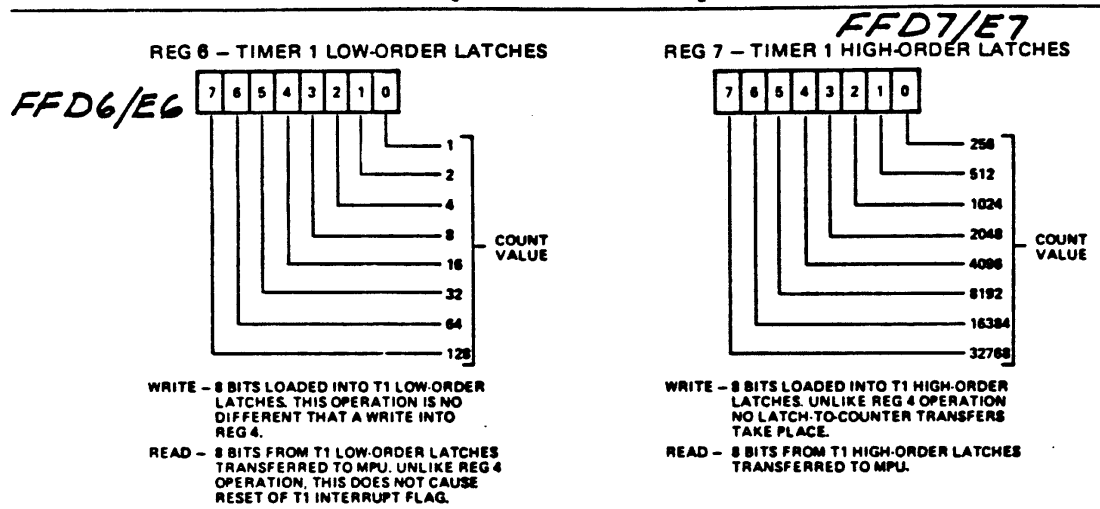



**Figure 16. T1 Latch Registers**

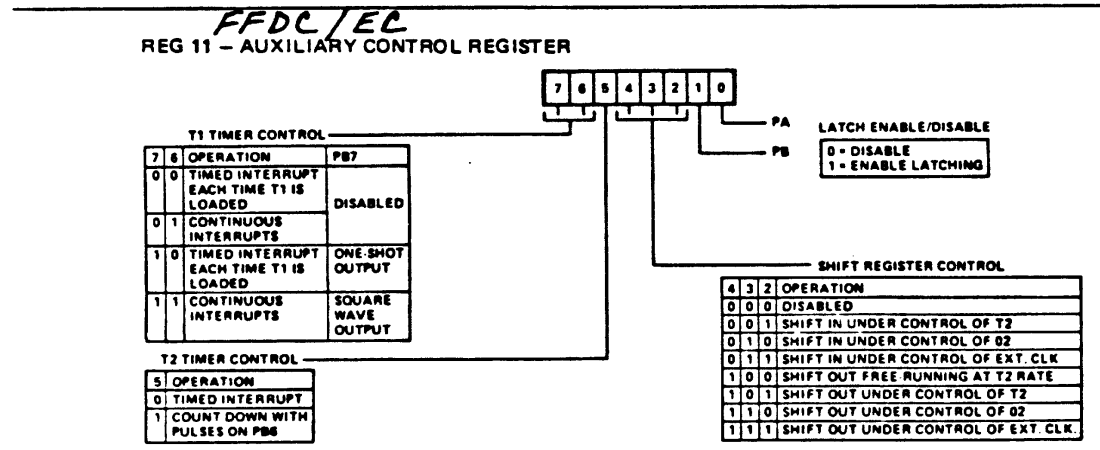
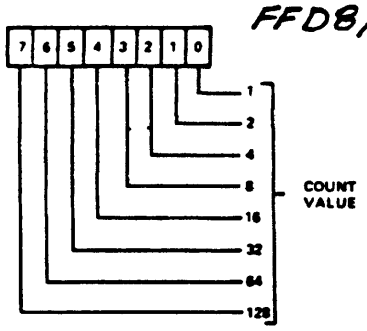



**Figure 17. Auxiliary Control Register**

Note: The processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

REG 8 – TIMER 2 LOW-ORDER COUNTER

FFD8/E8

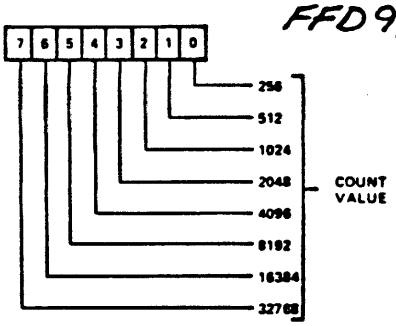



WRITE – 8 BITS LOADED INTO T2 LOW-ORDER LATCHES.

READ – 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

REG 9 – TIMER 2 HIGH-ORDER COUNTER

FFD9/E9

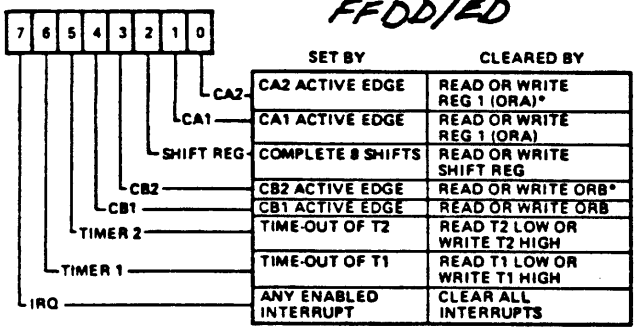



WRITE – 8 BITS LOADED INTO T2 HIGH-ORDER COUNTER ALSO, LOW-ORDER LATCHES TRANSFERRED TO LOW-ORDER COUNTER IN ADDITION, T2 INTERRUPT FLAG IS RESET.

READ – 8 BITS FROM T2 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

REG 13 – INTERRUPT FLAG REGISTER

FFDD/ED

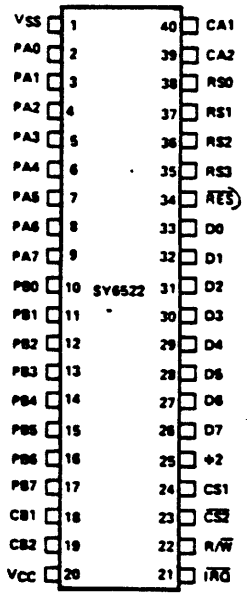



| | SET BY | CLEARED BY |
|---|---|---|
| CA2 | CA2 ACTIVE EDGE | READ OR WRITE REG 1 (ORA)* |
| CA1 | CA1 ACTIVE EDGE | READ OR WRITE REG 1 (ORA) |
| SHIFT REG | COMPLETE 8 SHIFTS | READ OR WRITE SHIFT REG |
| CB2 | CB2 ACTIVE EDGE | READ OR WRITE ORB* |
| CB1 | CB1 ACTIVE EDGE | READ OR WRITE ORB |
| TIMER 2 | TIME-OUT OF T2 | READ T2 LOW OR WRITE T2 HIGH |
| TIMER 1 | TIME-OUT OF T1 | READ T1 LOW OR WRITE T1 HIGH |
| IRQ | ANY ENABLED INTERRUPT | CLEAR ALL INTERRUPTS |

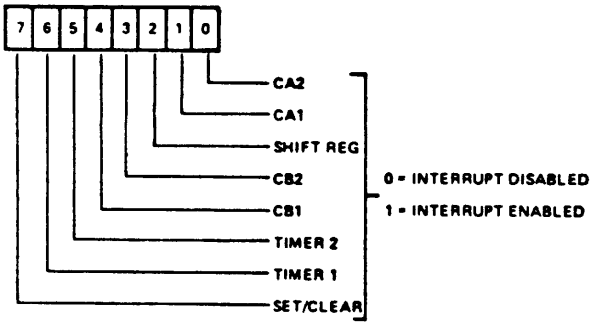
* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY.

**Figure 25. Interrupt Flag Register (IFR)**

PIN CONFIGURATION




REG 14 – INTERRUPT ENABLE REGISTER




NOTES:
1. IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0 - 6 DISABLES THE CORRESPONDING INTERRUPT.
2. IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0 - 6 ENABLES THE CORRESPONDING INTERRUPT.
3. IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "0" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.