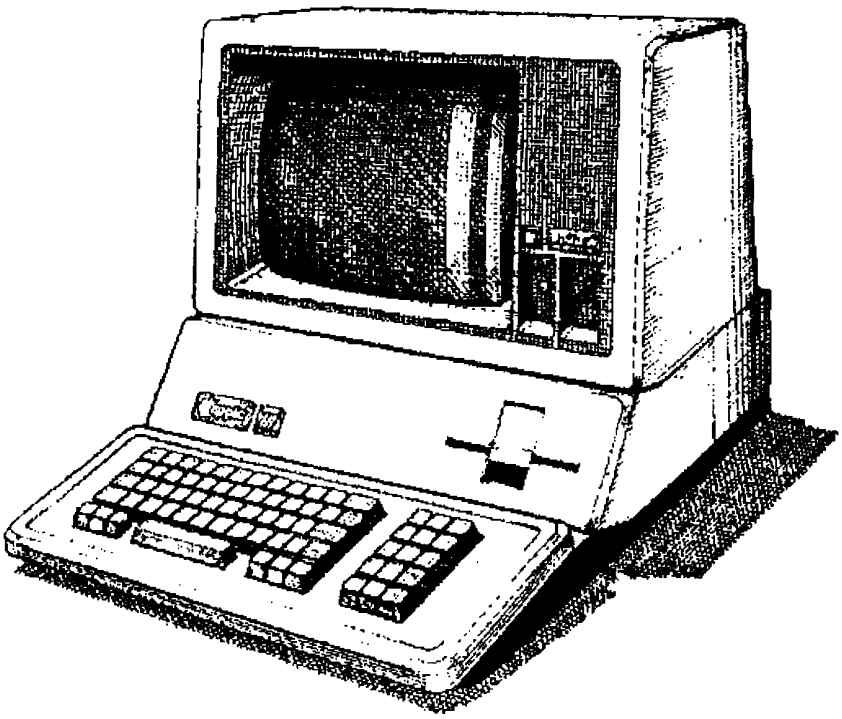
Apple /// Computer Information

Apple /// Service Reference Manual



Section I of II • Theory of Operation

Chapter 7 • Input / Output

Written by Apple Computer • 1982

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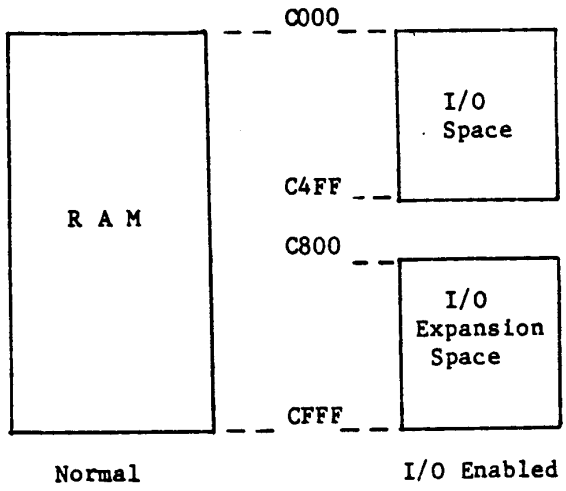
INPUT/OUTPUT (I/O)

DESCRIPTION

In Apple computers I/O devices are treated very much like memory locations. Most of the system's I/O functions are mapped into the address range C000 to CFFF. The I/O space is enabled by a bit in the Environmental Register. Addresses C0XX control the on-board I/O. Addresses C1XX, C2XX, C3XX, and C4XX are reserved for the exclusive use of the four I/O slots. The I/O expansion space from C800 to CFFF is switched between the I/O slots. Addresses C500 to C7FF are always Ram, regardless of the setting of the I/O enable bit.

I/O ADDRESS SPACE



INTERFACE CONTROL SIGNALS

For every I/O slot, the Apple /// provides 16 locations that set the Device Select* signal and 256 locations that set the I/O Select* signal.

The Device Select* signal is a signal specific to each slot. It is active for for a 16-address block. This signal is ususally used as an enable signal.

The I/O Select* signal can be used to control a page of memory (256 addresses) which could be placed in ROM, in the interface circuitry, for executing "driver routines". The I/O Select* signal could also be used in circumstances where a small amount of read/write memory for temporary storage is needed. Each I/O slot has its own I/O Select* signal, and each signal is active when a specific page of memory is addressed.

The I/O Strobe is common to all I/O slots. This signal will be low (true) when an address location within the range of C800 to CFFF (2K of memory).

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INTERRUPTS

Interface cards that are capable of generating interrupts MUST latch the interrupt output until it is reset by the software. In addition, they MUST include the ability to mask and unmask their interrupt through software, and MUST default to the masked state when the system is reset.

C09X	Slot 1 Device Select
C1XX	Slot 1 I/O Select
C0AX	Slot 2 Device Select
C2XX	Slot 2 I/O Select
C0BX	Slot 3 Device Select
C3XX	Slot 3 I/O Select
C0CX	Slot 4 Device Select
C4XX	Slot 4 I/O Select

The method of accomplishing this transmission between the interface and the computer is called handshaking. In the Apple ///, the handshaking is normally accomplished through the exchange of Device Select*, I/O Select*, IRQ*, and R/W*. The R/W* control signal is used to synchronize the flow of data to and from I/O devices. When the Read/Write* signal is a logic one, the processor is reading information from the data bus. Conversely, when R/W* is low, we are performing a write to the data bus.

As you can see, the handshaking between the Apple /// and the interface is dependent upon the software. Let us again emphasize the role of addressing plays in the I/O process.

ADDRESSING THE I/O

There are certain addresses that you can write to or read from to control the operation of the interface card. Where "n" is the number of the slot where the interface is installed, these hardware addresses are in the range:

C080 + n0 to C087 + n0

For example, if you install an interface in slot 2, you should write to the addresses from C0A0 through C0A7.

The operations that the interface card performs are initiated by the read or write operations presented on these hardware addresses.

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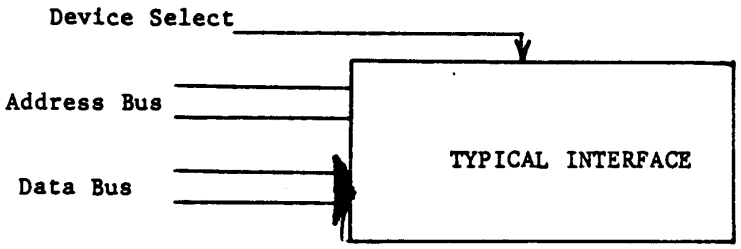
THE INPUT OPERATION

In the input operation, whenever the correct address is presented to the interface card, the data is present on the data lines D7-D0. For example, if the location C083 + n0 corresponds in the software to an input, the data presented on D7-D0 is accepted by the computer. If the interface card contains a control ROM, the code in ROM is being addressed whenever the I/O Select line is low; that is when the address on the address lines is between Cn00 and CnFF). Recall that "n" is the slot number.

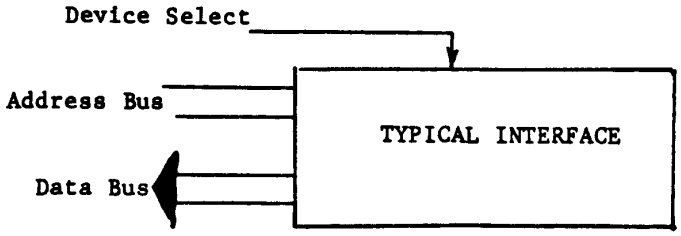


THE OUTPUT OPERATION

In the output operation,

IF the address Co81 + n0 represents an output operation in the software
AND the Read/Write* signal is low,

THEN the data is presented on the data bus and latched into the interface whenever the address C081 + n0 is presented.



SYSTEM TIMING

A system timing diagram is provided. This diagram shows the timing of some signals at the I/O slots in the 1 MHz and 2 MHz frequency modes.

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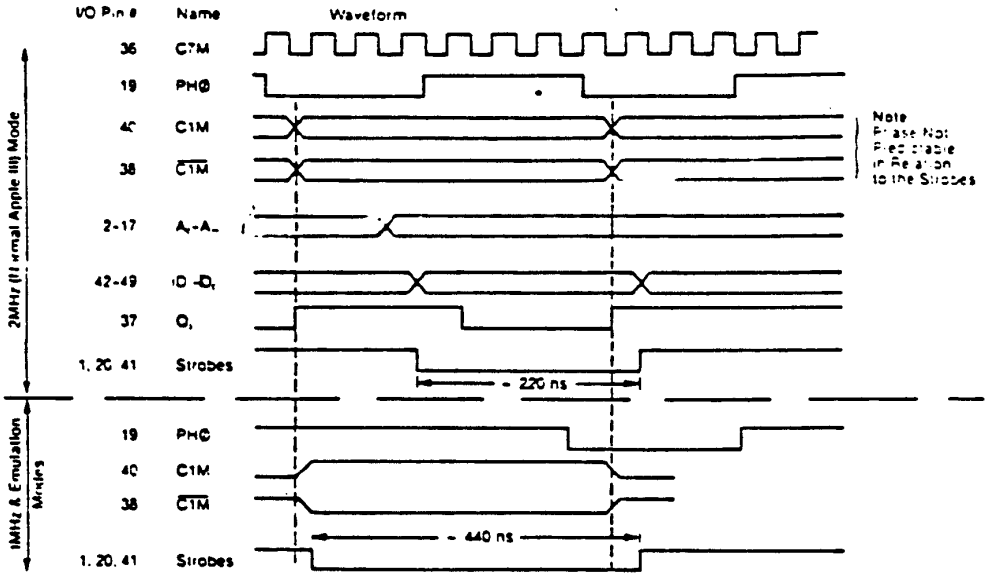
I/O TIMING DIAGRAMS



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THE A/// JOYSTICK

The A/// has two ports designated for joystick (x and y axis paddles) each with two switches. However, unlike the Apple II the ports do not have "annunicator" outputs. One of the switches is a momentary contact and the other is a toggle.

The Analog X and Y inputs are read through a ramp type Analog to Digital converter (A/D). These values derived must be interpreted by the program. The switches are read to the data bus directly through a mulitplexor.

The 9708 has multiplexed inputs. To select which input channel is to be read the proper address must be set in an addressable latch and must be held during the PDLEN (ramp start) low cycle.

The I/O address for the setting and clearing of the A/D addresses and the ramp start is as shown in the following table:

I/O Address	A/D Function	Signal Name
C058	A0 Clear	PDL0
C059	A0 Set	
C05A	A2 Clear	PDL2
C05B	A2 Set	
C05C	Ramp Start Clear	PDLEN
C05D	" " Set	
C05E	A1 Clear	AXC0
C05F	A1 Set	

To read the various signals associated with the joysticks the following addresses should be read:

I/O Address	Function
C060,8	Switch 0
C061,9	Switch 1/Margin Switch
C062,A	Switch 2
C063,B	Switch 3/Serial Clock
C066,E	A/D ramp stop (PDLOT)

Note: The joystick port at J3 (Port A) can be configured to be a serial port to support a device like the Silentype. Care must be taken to insure that the port has been configured for the proper device or signal contention will occur and give erroneous results.

The sequence of operation for the A/D would be as follows:

1) set the desired channel address nto A/D 0 through A/D 2.

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2) start the A/D by cycling the PDLEN signal low for 40 micro seconds then back high

3) set up one of the timers to count.

4) test for ramp stop

5) read the counter

6) compute the value of the channel input.

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Peripheral Connector Pinout

GND	26	25	+5V
DMAOK	27	24	NOT USED
$\overline{\text{DMAI}}$	28	23	NOT USED
$\overline{\text{IONMI}}$	29	22	$\overline{\text{TSADE}}$ (Open collector)
$\overline{\text{IRQ}}$	30	21	RDY (Open collector)
$\overline{\text{IORES}}$	31	20	$\overline{\text{I/O STROBE}}$
$\overline{\text{INH}}$	32	19	PHO
-12V	33	18	R/$\overline{\text{W}}$
-5V	34	17	A15
SYNC	35	16	A14
C7M	36	15	A13
Q3	37	14	A12
$\overline{\text{C1M}}$	38	13	A11
$\overline{\text{IOCLR}}$	39	12	A10
C1M	40	11	A9
$\overline{\text{DEV SEL}}$	41	10	A8
D7	42	9	A7
D6	43	8	A6
D5	44	7	A5
D4	45	6	A4
D3	46	5	A3
D2	47	4	A2
D1	48	3	A1
D0	49	2	A0
+12V	50	1	$\overline{\text{I/O SELECT}}$

A/// Peripheral Connector Slot

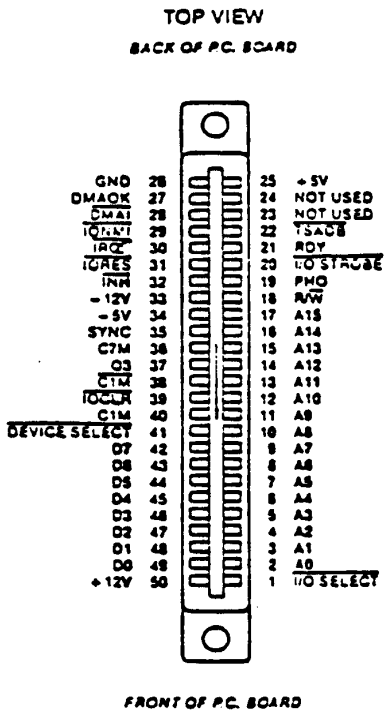

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Table 33: Peripheral Connector Signal Description

Pin:	Name:	I/O	Description:
1	$\overline{\text{I/O SELECT}}$	O	This line, normally high, will become low when the microprocessor references page $Cn, where n is the individual slot number. This signal become active during PH0 (nominally 500ns) and will drive 12 LSTTL loads.
2-17	A0-A15	I,O	The buffered address bus. The address on these lines becomes valid within 300ns after the beginning of $\overline{\text{C1M}}$ and remains vaild through PH0. These lines will each drive 8 LSTTL loads.
18	R/$\overline{\text{W}}$	I,O	Buffered Read/$\overline{\text{Write}}$ signal. This becomes valid at the same time the address bus does, and goes high during a read cycle and low during a write. This line can drive up to 10 LSTTL loads.
19	PH0	O	A 1 MHz signal which is identical to C1M. This line will drive 5 LSTTL inputs.
20	$\overline{\text{I/O STROBE}}$	O	This line will go low during C1M when the address bus contains an address between $C000 and $CFFF. This line will drive 12 LSTTL loads.
21	RDY	I	The 6502's RDY input. This line should change only during C1M, and when low will halt the microprocessor on the next read cycle. This line has a 1K ohm pullup to +5V. This line should be driven from an open collector output.
22	$\overline{\text{TSADB}}$	I	A low on this line from the peripheral will cause the address bus to tri-state for Direct Memory Access (DMA) applications. This has a 1 K ohm resistor pullup to +5V. This should be driven from an open collector output.
23		NA	Not used in an Apple ///(NO DAISY CHAINING OF PERIPHERALS!
24		NA	Not used in an Apple ///.
25	+5V	O	Positive 5-volt supply, 2.0 amps total for all peripheral boards together (but note a limit of 1.5 Watts per board).
26	GND	NA	System circuit ground. 0 volt line from power supply. Do not use for shield ground.
27	DMAOK	O	Acknowledge signal to the peripheral following

			its request for the special Direct Memory Access (DMA) mode. Informs the peripheral that the DMA can now proceed.
28	$\overline{\text{DMAI}}$	I	Direct Memory Access (DMA) interrupt. Requests the A Apple /// DMA mode. Has a 1 K ohm pullup to +5. This should be driven from an open collector output.
29	$\overline{\text{IONMI}}$	I	Input/Output Non-Maskable Interrupt. This is equivalent to the IORES (pin 31) line as it will execute the same code in the Autostart ROM. This line should be driven by an open collector output. THE NMI DOES NOT GO DIRECTLY TO THE PROCESSOR, SO IT CAN BE MASKED BY THE SYSTEM RESET FUNCTION.
30	$\overline{\text{IRQ}}$	I	This line is ignored in Apple][emulation mode. It should be driven by a TTL output.
31	$\overline{\text{IORES}}$	O	Input/Output Reset signal used to reset the peripheral devices. Pulled low by a power on or RESET key. This line will drive 12 LSTTL loads.
32	$\overline{\text{INH}}$	I	Inhibit line. When a device pulls this line low, all system memory is disabled. This line has a 1 K ohm pullup resistor to +5V and should be driven form an open collector output.
33	-12V	O	Negative 12 volt supply, 200mA total for all peripheral boards together.
34	-5V	O	Negative 5 volt supply, 200mA total for all periperal boards together.
35	SYNC	O	The 6502 opcode synchronization signal. Can be used for external bus control signals. Will drive 10 LSTTL loads.
36	C7M	O	Seven MHz high frequency clock. Will drive 10 LSTTL loads.
37	Q3	O	A 2MHz (nonsymetrical) general purpose timing signal. Will drive 10 LSTTL inputs.
38	$\overline{\text{C1M}}$	O	Complement of C1M clock. This will drive 12 LSTTL loads.
39	$\overline{\text{IOCLR}}$	O	Provides the $C800 space disable function directly without address decoding ($CFFF is used for Apple][peripherals. It is addressed from $C02x. This line will drive 12 LSTTL loads.
40	$\overline{\text{C1M}}$	O	Phase C1M clock. This is the same as the microprocessor's 1 MHz clock. This will drive 12 LSTTL loads.
41	$\overline{\text{DEVICE SELECT}}$		This line becomes acive (low) on each peripheral

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			connector when the address bus is holding address between $C0n0 and $C0nF where n is the slot number plus $8. This line will drive 12 LSTTL loads.
42-49	D7-D0	I,O	The 8-bit system data bus. During a write cycle, data is set up by the 6502 less than 300ns after the beginning of $\overline{C1M}$. During a read cycle the 6502 expects data to be ready no less than 100ns before the end of $\overline{C1M}$. These lines will drive 8 LSTTL inputs.
50	+12V	O	Positive 12 volt supply*, 300mA total for all peripheral boards together.

* NOTE: TOTAL POWER DRAWN BY ANY ONE PERIPHERAL CARD IS NOT TO EXCEED 1.5 WATTS

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The Real Time Clock/Calendar

A real time clock has been incorporated into the A /// using 58167 CMOS Clock/Calendar chip. This chip has the resolution to count to thousandths of a second. The clock circuitry can be set to cause an interrupt at intervals from a tenth of a second to interrupts every month.

Since the clock is a CMOS circuit it consumes about 10ua in the standby (power off in the Apple ///) mode. This is about the same as a normal LCD watch. Three "AA" alkaline batteries are mounted in a battery pack that clips to the casting near the internal speaker. Wires attached to the battery holder connect to a 2 pin molex connector at location G13.

This clock chip is not a member of the 6500 family and is not directly compatible. Special considerations have been incorporated into the logic design to allow the Apple III to access and control of the clock chip.

The timing requirements for the clock chip require that the address lines be latched for much longer than the processor can accomplish in normal operations, so the clock is addressed with the "Zero Page Register" (the B port of VIA B6). The operating system will temporarily store the current zero page address at another location then write the desired clock address into the zpage register. The processor clock, PH0, is extended to --usec by the action of the prom 180 and associated circuit. The clock chip also requires a separate read and write strobe so appropriate logic was designed to split the R/W signal into a read and write strobe.

When the processor has completed its access to the clock it will return the proper zero page address to the VIA and PH0 will return to its normal operation.

Please refer to the specification sheet in the Appendices for complete details of the clock.

The transistor array performs two functions. One it supplies Vcc from the power supply when the Apple /// is "on", and develops a power down strobe to the clock chip to set its standby mode just before the supply fully decays.

The clock may be programmed that while it is in the standby mode to provide a PDINT to an external device which may restore power to the Apple to service a particular device. This feature would be very useful in communications networks that poll at specific times in off-hours. However, at the time of this printing no such remote device has been specified.

The clock runs on a 32KHZ crystal may be adjusted to an operating tolerance of 5 minutes a month. There are two methods used, on is a vertifications of operation using software, this however has the accuracy of approximately 5 minutes a month, which for many applications and users is close enough, but for those users who demand a closer setting a method of setting the clock using an accoustic probe and frequently meter is available. The only problem with this is the cost of the calibration equipment (nearly $1000 per station). Level II centers will most likely be equipped with these devices.

It should be noted that there is a slight shift if frequently between power on

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and standy modes. Depending on the actual usage of power on and off the clock may vary perceptibly over the course of a month. So it is best to describe the entire function as a clock, not a chronograph.

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