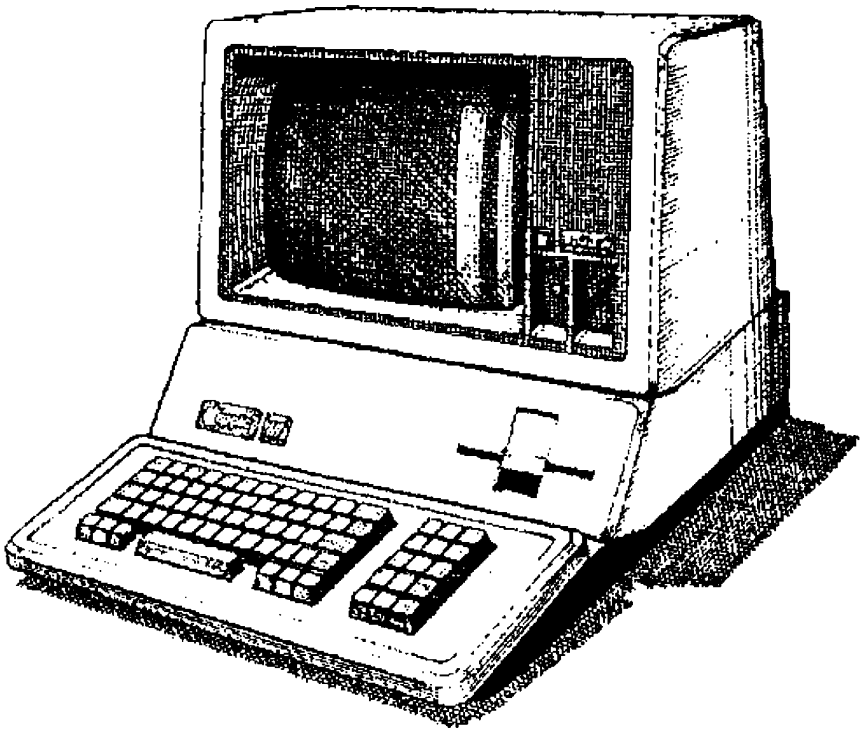
Apple /// Computer Information

Apple /// Service Reference Manual



Section I of II • Theory of Operation

Chapter 12 • Floppy Disk Subsystem

Written by Apple Computer • 1982

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THE DISK /// SUBSYSTEM

I THEORY OF OPERATION

The Disk /// subsystem, is a self contained Apple /// peripheral which allows user programs and data to be stored and retrieved on 5 1/4" floppy diskettes. The Apple /// supplies DC power, control signals, and a parallel data path to the Disk /// via the A///s main logic board Disk Conditioner (Controller) Circuit. The Disk Conditioner sends DC power, control signals, and serial data to the Analog Card via a 26-conductor ribbon cable.

The Analog Card contains disk read-write electronics, drivers for positioning Stepper Motor, and a transistor power switch. Analog Card also contains circuitry which causes its output signals to the disk conditioner circuit to be active only when the card is enabled. This allows up to 4 Analog Cards to share the same data path for a 4 drive system (one internal, three external drives).

Within the drive itself, movement of Stepper Motor rotates Actuator Cam. Head and Carriage Assembly's Cam Follower, rides in Actuator Cam's spiral groove. Two Guide Rods allow motion of Head and Carriage Assembly either towards, or away from Drive Door. This positions Read/Write Head to appropriate track, so that serial data may then be transferred to and from disk using high-level commands.

A - DISK CONDITIONER CIRCUIT

There are seven sections in the Disk Conditioner circuit:
(Refer to Schematic of Disk Conditioner Logic)

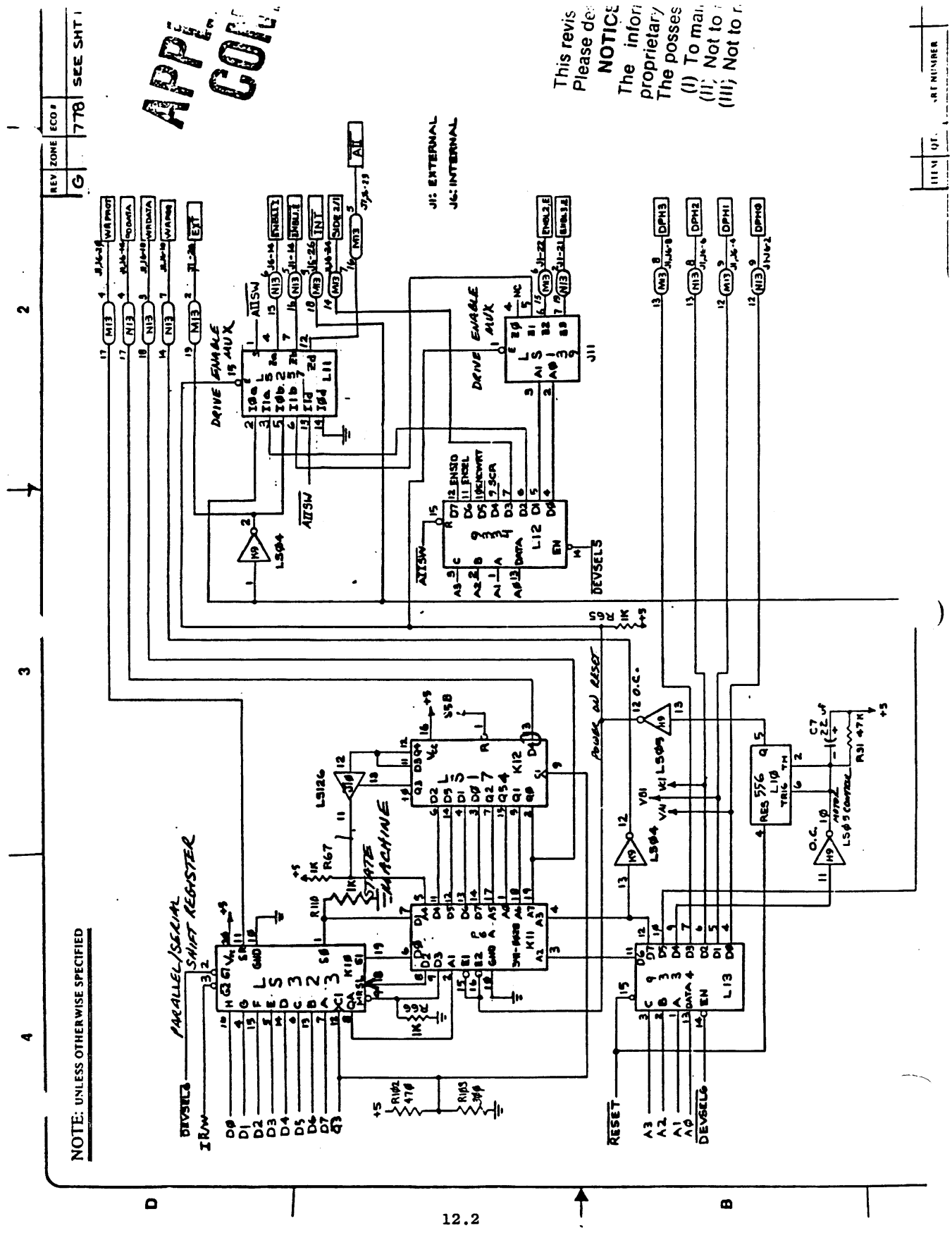
1. Power-On Reset

   This circuit consists of one half of 556 Timer and one open-collector inverter. When power is applied, the outputs of the 9334/LS259 Address Latch (DPh0-3) are brought low which places the Disk Conditioning logic in the read mode, the Q output of the 556 timer (pin 5) goes high for about 65 ms, bringing inverter's output to ground. This resets the State Machine (Prom P6A), and the Drive Enable Multiplexers. The drive enable multiplexer's Z output is prevented from enabling the internal and external drives.

2. The BOOT ROM

   The Boot ROM, though not a part of the disk conditioning circuit, contains the routine which down loads the operating system (SOS) from disk and then jumps into it. The LS323, an 8 Bit Parallel/Serial Register, is enabled (DEVSEL6*) whenever the address C0Exxn is presented. the data, from the boot rom, is converted to serial at the output of pin 1 in the 74LS323 in a write operation.

3. Addressable Latch (9334 or 74LS259).


NOTE: UNLESS OTHERWISE SPECIFIED
PARALLEL/SERIAL SHIFT REGISTER
STATE MACHINE
DRIVE ENABLE MUX
J1: ENTERNAL
J6: INTERNAL
DEVSEL5
DEVSEL6
RESET
IRW
ATSW
INT
ENT
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This chip provides an eight software-controlled output. When DEVSEL6* (pin 9 of LS138 I/O Address Decoder) signal goes low (one of 16 addresses starting at [C0Exxn†, value of Address Line A0 becomes the new value of D output pointed to by Address Lines A1-A3. Latch output D6 and D7 set operating mode of controller (read, write, etc). Q5 selects the internal drive. D4 controls MOTOR ON signal and D0 to D3, set position of the Stepper Motor. Drive enable signals ENBL1I and ENBL1E are true when MOTOR ON signal is true and appropriate drive is selected.

4. State Machine (PROM P6A and 74LS174)

These two parts contain nucleus of Disk Conditioning Logic. A State Machine is a device capable of storing a value in a register. That value, in conjunction with external input, determines what the next register value should be and what output should be generated. Value in register is, machines's Current State and next value is machine's Next State. State machine updates at each clocking, going from state to state and producing output base on state its in and value of its input just before clocking.

Current State, is value at Q2, Q5, Q1, and Q0 from 74LS174. Next state is value of D4-D7 from P6A PROM. Input to State Machine includes D6 and D7 from 9334, QA* output from 74LS174 Shift Register and A2-11. Output from State Machine is PROM signals D0-D3, which effect Shift Register. Q0 from 74LS174, which is high-order bit of Current State, forms WR DATA output. Since State Machine is clocked by two Megahertz Q3* signal, the state lasts for 500 ns.

Flux transitions on diskette are detected by Analog Card and are sent to Disk Conditioning Circuitry as RD DATA. These one microsecond positive going pulses appear at D4 input to 74LS174. NAND Gate and Inverter, which connect to 74LS174's Q3 and Q4 output, cause A4 input to P6A PROM to go low for one state following the falling edge of RD DATA. This information is ignored when writing out to disk. When reading from disk, however, this input forms the basis for determining whether a logic one or zero has been read. A logic one is indicated by a four microsecond period. A logic zero, by an eight microsecond period between flux transitions.

5. Shift Register

74LS323 Universal 8 Bit Parallel/Serial Shift Register, transfers data to and from the Apple ///. When writing to disk, Shift Register under control of State Machine, parallel loads a data byte from the A/// and shifts it left. This causes QA* output to effect State Machine's A1 input. State Machine goes through a different state sequence for a logic one and a logic zero, which causes WR DATA to change value every four and eight microseconds, respectively.

When reading from disk, State Machine shifts appropriate logic levels into Shift Register's SL input. Resulting byte can be read by the A///.

Status of Write Protect switch in Disk Drive, comes into SR input of

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Shift Register from Analog Card. Under control of State Machine, Shift Register is placed into a shift right mode, allowing status of switch to be read by software.

6. MOTOR ON Circuit.

Q output from one half of 556 timer, forms MOTOR ON signal. MOTOR ON becomes true when B2-6 is brought to ground under software control. An enable is sent to one of the drives, and Drive Motor in selected drive turns on. When software causes B2-6 to become high-impedance in order to turn off drive, C7 and R31 give drive a 2/3 second grace period before MOTOR ON times out. This prevents drive from being turned on and off when repeated accesses are made.

7. AII EMULATION MODE

With the AIISW* true and DEVSEL5* (addressed by CODxxn) selected, the internal and external drives are fooled into operating as an Apple II Disk Drive.

B - ANALOG CARD (Refer to Analog Card Schematic Diagram)

1. Enable Circuit

A Disk Drive connected to the Apple /// is always in one of three operating modes:

a - Read Mode

Flux transitions on diskette are detected by MC3470P Floppy Disk Read Amplifier on Analog Card and are sent to the Disk Conditioner as one microsecond positive-going pulses across RD DATA* line.

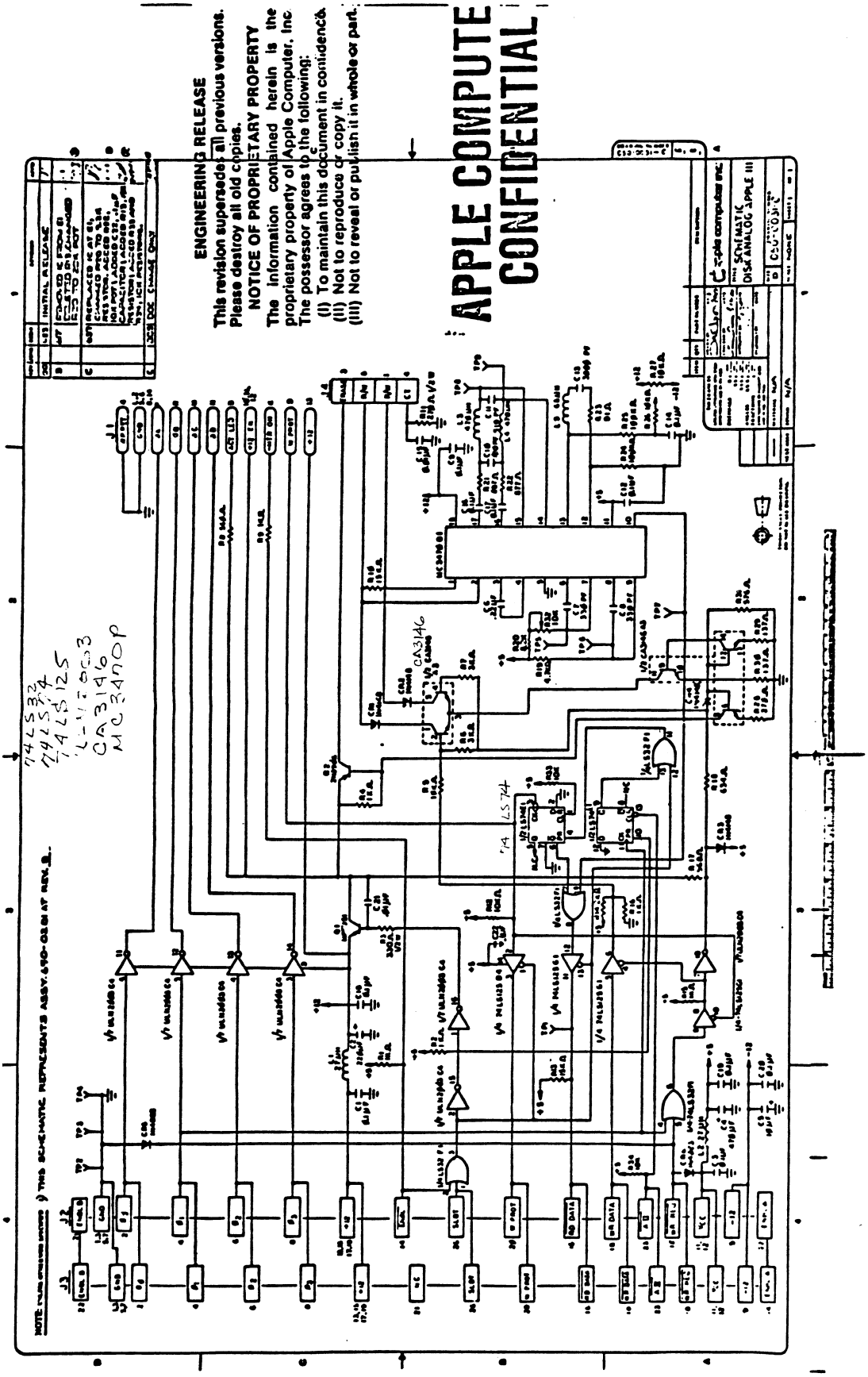
b. Write Mode

Here WR DATA input to Analog Card determines polarity of write current passing through head.

c. Deselected Mode

In this state, drive is not currently performing any data transfers with the Apple ///.

A drived becomes enabled, when ENBL1I input to the Analog Card on the selected drive goes low. This causes Q1 to turn on because current flows through R3 into pin 16 of ULN2003's Darlington output. +12 volts is then supplied to Stepper Motor. Q1 also provides a power source for Write and Erase Current circuits. In addition, ENBL1I signal also enable RD DATA* and W PROT tristate buffers and supplies a MTR ON control signal to Motor Control Board through resistor R9.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SCHEMATIC
DISK ANALOG APPLE III
74LS32
74LS74
74LS125
74LS03
CA3146
MC3470P
74 LS74

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d. Read Electronics

MC3470P Floppy Disk Read Amplifier and associated discrete components, provide a one-chip interface between magnetic head of Disk Drive and RD DATA* input to Disk Conditioning circuit of the main logic board. MC3470P contains both analog and digital circuits which cause a TTL compatible pulse to be generated for each positive and negative peak of input signal.

Input voltage from head appears across pins 1 and 2 of MC3470P. This signal passes through an amplifier and is differentially applied to a noise filter made up of R21 and R22, C10 and C11 and L3 and L4. Filter's output feeds back into MC3470P, where a differentiator circuit provides an output proportional to rate of change, with time, of input signal. In addition, a 90 degree phase lead is introduced which causes a zero crossing at differentiator's output to correspond with a peak at its input. L5, C13 and R23 determine characteristics of differentiator. R27 allows for correction of current imbalances within differentiator so that a sinusoidal input waveform produces evenly spaced RD DATA* pulses.

Zero crossings at output of differentiator cause output of a comparator within MC3470P, in conjunction with digital circuits, create a Time Domain Filter which checks against false zero crossing readings due to distored input waveforms or noise. When a zero crossing is detected, mono #1, formed by R20, R32, and C7, is triggered. At end of its two microsecond period, output of comparitor is again checked. If it has not changed (valid zero - crossing), mono #2 gets a trigger pulse that uses R19 and C8 to generate one microsecond RD DATA* pulse at pin 10 of MC34709P.

3. Write Electronics

During Read Mode (WR REQ* high), ULN2003 Darlington output at C4-10, is close to ground potential. This prevents erase current switch Q2 from turning on and disables write current return path. During Write Mode, the anode of CR3 is pulled up to +5.7 V. Q2 receives base current through A3-8, and provides current to erase coil of head. R11 serves as return for erase current, which is roughly 44 milliamps. Erase coil in head straddles both sides of read-write head, preventing write current from spreading into adjacent tracks on diskette.

When writing out to diskette, flux transistions are placed on surface of diskette by changing polarity of current flow in head's read-write coil. Write current enters read-write coil through its center tap, which is connected to return side of erase coil. Two of CA3146's transistors connected to R29 and R30 form a current mirror which drives pin three of CA3146.

This establishes write current return path. When writing out to disk, WR DATA causes a differential voltage to be applied to pins 2 and 4 of CA3146, which causes a differential current flow in write coil. Each polarity reversal places a flux reversal on

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diskette. (Current in R/W coil -6.8 ma P-P)

4. Write Protect Circuit

Ananlog Card only allows erase and write current to be generated when diskette has its write protect notch uncovered. If notch is absent (write protected), the Write Protech switch is held open even though diskette is fully inserted into drive. This causes pullup resistor R12 to disable G1-8, which causes WR REQ* signal to be pulled up to a false level by R15. This prevents write current mirror from supplying write current to head. Write Protect status is ent to Disk Conditioning circuitry on Main Logic board as W PROT.

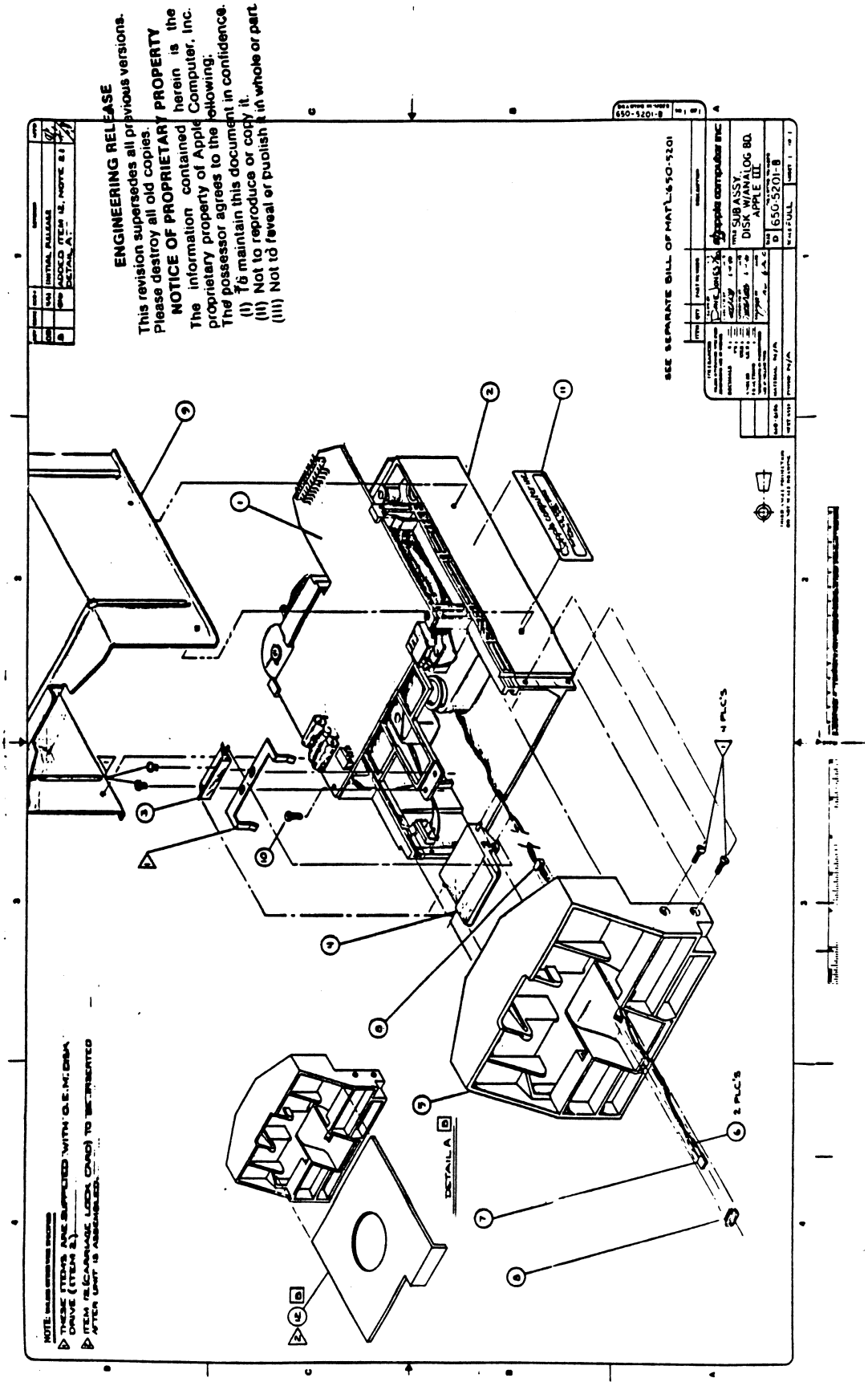
If Write Protect notch has been uncovered, it cause Write Protect switch within drive to close. Phase 1 signal from the Disk Conditioning circuitry provides return path for current passing through switch. If Phase 1 signal is high, it indicates that Stepper Motor is in one of its two transient states between tracks. Write Protect circuits behave as they do when the diskette is write protected. This provides partial coverage against writing when Stepper Motor is off track.

5. Stepper Motor Drivers

A ULN2003 Darlington Buffer-Inverter, provides a current return path for each of four Steper Motor windings, Phase A through Phase D. Q1 provides windings with source current when dirve is enabled. Since input to each ULN2003 stage is provided by the Disk Conditioning circuit's 9334 Addressalbe Latch output, Stepper Motor is then under software control.

Stepping in from Track 0 towards Track 34 (towards hub), requires Stepper Windings to be energized in Phase A, B, C, D order. Each phase rotates Cam Follower enough to provide one-half track movement of Head and Carriage assembly. Phase Ad and C are energized when head is on track, and Phase B and D are between track positions. Once head is positioned to desired track, power is removed from Stepper Motor to reduce power consumption.

Stepping out requires Stepper Motor windings to be enegized in Phase D, C, B, A order. When booting, windings are pulsed enough times to guarantee that head is positioned over Track 0.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SEE SEPARATE BILL OF MAT'L 650-5201
SUB ASSY, DISK W/ANALOG BD, APPLE III
650-5201-B
4 PLC'S
2 PLC'S
DETAIL A

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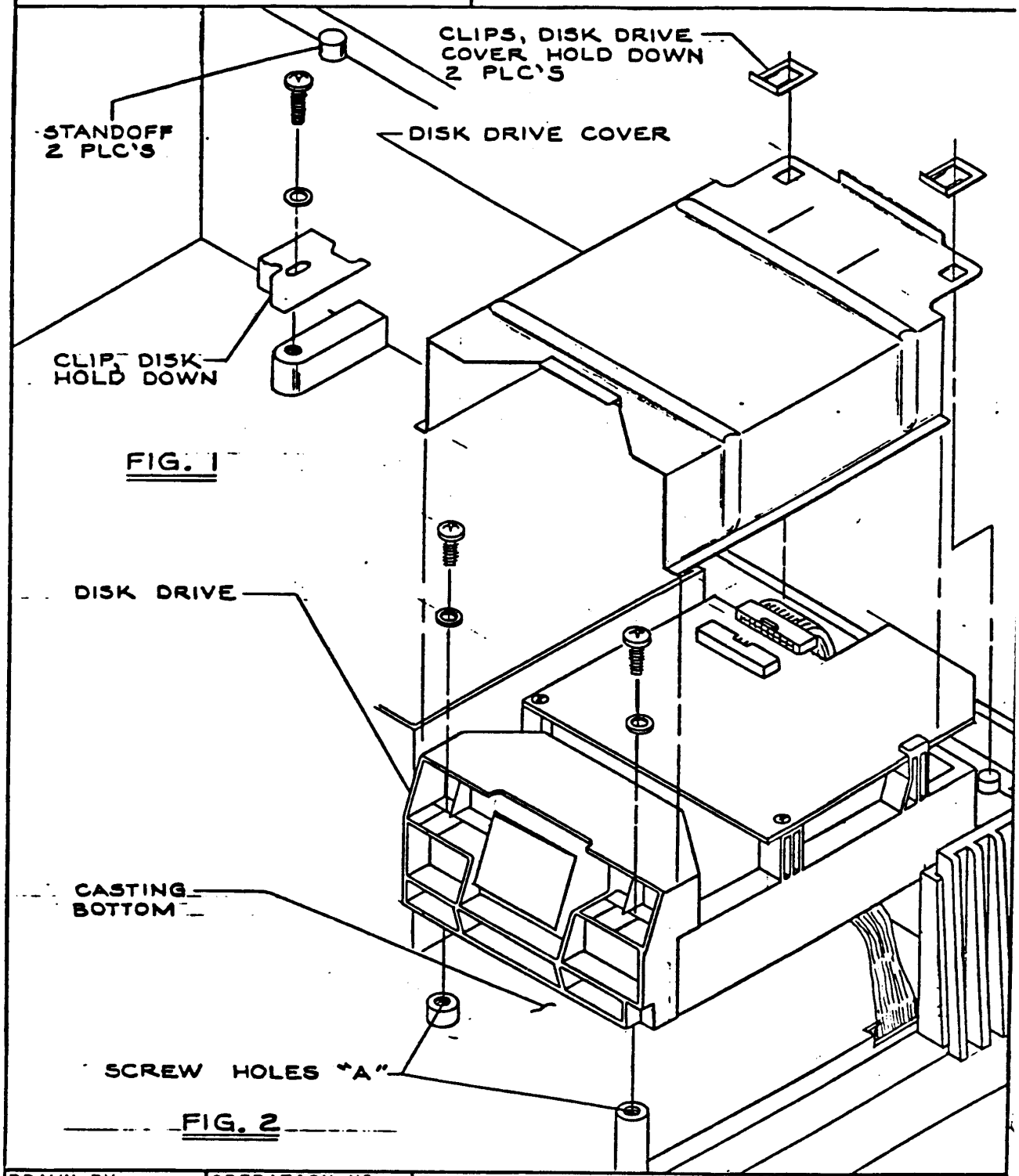

FIG. 1

FIG. 2

DRAWN BY	OPERATION NO.	TITLE
C. Latter	010	INSTALL DISK DRIVE

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APPLE III

DISK ENABLE(S)

1) TO ENABLE THE INTERNAL DRIVE 1, THE FOLLOWING CODE SHOULD BE TYPED IN: $\overline{C\phi EA}$ @ PIN #10 (L13)

2) TO ENABLE THE $\overline{\text{EXT.}}$ DRIVES (1,2,OR3), THE FOLLOWING CODE MUST BE TYPED IN:

$\overline{C\phi EB}$ @ PIN #10 (L13)

3) THE FOLLOWING TRUTH TABLE WILL EXPLAIN HOW DRIVES ($\overline{\text{INT}}$ AND $\overline{\text{EXT}}$) *ϕ, 1, 2 AND 3 ARE ENABLED

*ϕ ≡ INT. DRIVE

	DRIVE#	CODES TO TYPE IN	ENABLE	A1	Aϕ	Zϕ	Z1	Z2	Z3	➡ FROM J11 (LS)
			1	DON'T CARE	DON'T CARE	1	1	1	1	
1I	ϕ	CϕD4, CϕD2, C$\phi\phi\phi$	ϕ	ϕ	ϕ	ϕ	1	1	1	★
1E	1	CϕD2, CϕD1	ϕ	ϕ	1	1	ϕ	1	1	★
2E	2	CϕD3, C$\phi\phi\phi$	ϕ	1	ϕ	1	1	ϕ	1	PIN #6 J11 (LS139)
3E	3	CϕD3, CϕD1	ϕ	1	1	1	1	1	ϕ	PIN #7 J11 (LS139)

★ ≡ COINCEDENTAL LOGIC LEVELS.

4) CϕE9 WILL ENABLE J11 (LS139), HENCE THE APPROPRIATE DRIVE WILL BE ENABLED.

EXAMPLE:

LETS ENABLE DRIVE #2

A) TYPE IN THE CODE : CϕEB

B) TYPE IN THE CODE : CϕD3 AND C$\phi\phi\phi$

C) TYPE IN THE CODE : CϕE9 NOW DRIVE #2 IS ON

D) TYPE IN THE CODE : CϕE8 NOW DRIVE #2 IS OFF. S. WOZ 281