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## WARRANTY

Zip Technology warrants the internal circuitry of this product to be in good working order for the lifetime of the original registered purchaser. Should the internal circuitry of this product fail, after having been properly installed as directed in the Instruction Manual, ZIP Technology will replace it with another ZIPCHIP. This warranty does not imply that any broken chip or any chip suffering a broken pin from improper installation, will automatically be replaced. ZIP Technology is constantly working to improve its products and may, at its option, perform warranty replacement with a later version of the product.

To obtain a replacement for a non-functioning ZIPCHIP call ZIP Technology's Customer Service Department to obtain a Return Merchandise Authorization number(RMA). Proof of purchase will be required before a RMA number will be issued. No merchandise will be replaced unless the non-functioning chip is returned accompanied by an RMA number. All shipping and insurance costs must be the responsibility of the person returning the product. All replaced products become the property of ZIP Technology.

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This manual was designed, written and illustrated by Russ McCaffrey.

ZIP Technology may make improvements and/or changes to the product described in this manual at any time without notice. All information presented here has been carefully checked by technical personnel, however ZIP Technology makes no guarantee concerning the validity or completeness and will not be responsible for the use thereof. Changes are periodically made to the information herein. These changes will be incorporated in later editions of this publication.

ZIP Technology recommends that the owner make a backup of the ZIP Utility disk, and use the backup for normal work.

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# ZIP CHIP™ INSTRUCTION MANUAL

# INTRODUCTION

The Zip Technology **ZIP CHIP** is a speed-up card on a chip for the Apple // Plus, Apple //e and the Apple //c computers and compatibles. The chip replaces the standard 6502 or 65C02 processor (CPU) chip in the Apple and provides user selectable High/Low speed operation. The sound to the speaker and the interaction of the joystick can be speeded up also.

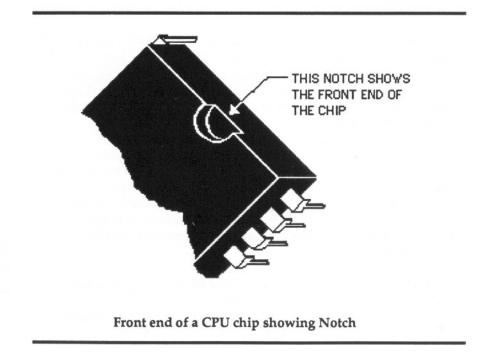
The **ZIP CHIP** runs with all existing Apple Hardware peripherals (except some of those that use Direct Memory Access [DMA]) and all Apple software that will currently run on the particular Apple model. Those hardware and software items that physically can run at high speed are enabled to do so. Those that cannot run at high speed can still be used at their normal speed...even with the **ZIP CHIP** in place.

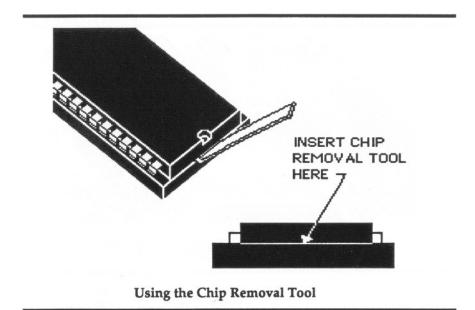
Each individual slot in the Apple is enabled for High or Low speed. The user can accept the default slot settings or through supplied utilities, set each slot for high or low speed. This allows for printers, modems, disk drives, CP/M cards and other special cards.

The operating speed of the **ZIP CHIP** can also be changed from nearly half normal Apple speed to four times normal speed in eighteen increments. High Speed operation of the chip can even be entirely defeated by the user at startup time.

Hundreds of programs and dozens of peripheral units and boards have been used with the **ZIP CHIP**. However, if the user encounters any specific problem, **Zip** Technology maintains a Customer Service Hotline.

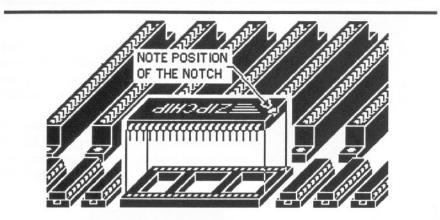
The following instructions will assist the user in the installation of the **ZIP CHIP**, use of the chip, use of the utility programs and programming instructions for incorporating the features of **ZIP CHIP** in new software.





# CHIP REMOVAL TOOL USE

A Chip Removal Tool is supplied free with your **ZIP CHIP**. This tool will enable anyone to easily remove the 6502 or 65C02 CPU chip to replace it with the **ZIP CHIP**. The short end of the tool is wedged between the CPU chip and the socket as shown in the above illustration. If there is a problem inserting the tool between the CPU chip and the socket, use a fine pointed screwdriver to begin prying up the chip. While holding the bottom of the tool in, put a gentle pull on the long end. This will pry the CPU chip. Once the chip is lifted mostly out of the socket, it can be then lifted by hand. Take care not to bend any of the pins of the CPU chip. Put it in a safe place. Note: Retain your Zip Chip Removal Tool. While it was designed specifically for removing CPU chips, you will find it useful for other tasks.



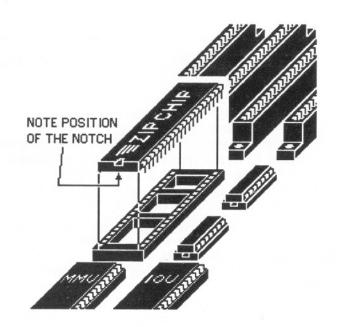
Installing ZIP CHIP in an Apple // Plus

### INSTALLATION

Installing the **ZIP CHIP** in an Apple // Plus - Installing **ZIP CHIP** in a // plus is a simple step by step process:

- 1. Turn off all power to the Apple
- 2. Remove the cover from the computer.
- 3. Carefully remove any peripheral boards that prevent easy access to the 6502 or 65C02 CPU chip. This chip is located on the motherboard on row H, columns 6 through 9. It is the largest chip in the Apple // Plus. The front of this chip (the end with the notch) is to the right.
- 4. Slide the short end of the supplied Chip Removal Tool into the slot between one end of the CPU chip and its socket. Take care NOT to get the tool under the socket.
- 5. Gently rock the long end of the tool prying the end of the CPU chip from the socket.
- 6. Do the same thing to the other end of the CPU chip.
- 7. Lift the 6502 or 65C02 CPU chip out of the computer and put it in a safe place.
- 8. Take the **ZIP CHIP** and place it over the empty socket. Be sure that the notched end of the chip is to the right.
- 9. Slowly press the **ZIP CHIP** down into the socket. Be sure that all the pins are going into socket holes.
- 10. When the chip is in place, firmly press down on each end to "seat" the chip.
- 11. Replace any boards you may have removed and replace the cover of the computer.

CONGRATULATIONS! You have now installed the ZIP CHIP! You may now proceed to the chapter on USE OF THE ZIP CHIP.

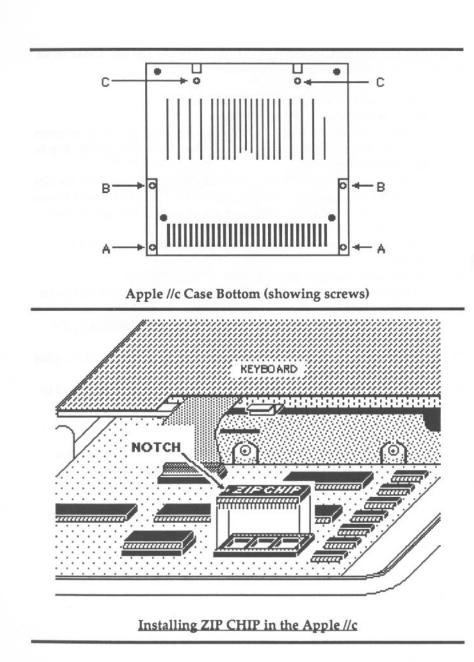


## Installing ZIP CHIP in an APPLE //e

Installing the **ZIP CHIP** in an Apple //e - Installing the **ZIP CHIP** in an Apple //e is a simple step-by-step process.

- 1. Turn off all power to the Apple Computer.
- 2. Remove the cover from the computer.
- Locate the 6502 or 65C02 CPU chip. It is located on row B, column 4 and is the long chip nearest the slot row. The front of this chip is towards the keyboard.
- 4. Slide the short end of the supplied Chip Removal Tool into the slot under the front end of the exiting 6502 or 65C02 CPU chip between the chip and the socket. Take care not to get the tool under the socket itself.
- Rock the long end of the tool gently prying the chip from the socket.
- 6. Do the same thing to the other end of the CPU chip.
- 7. Grasp the chip and gently remove it from the computer and put it in a safe place.
- Take the ZIP CHIP and hold it so that the notched end faces the keyboard. Lower the chip to the socket.
- 9. Slowly press the **ZIP CHIP** into the socket. Be sure that all the pins are going into socket holes.
- 10. When the **ZIP CHIP** is in place, firmly press down on each end to "seat" the chip.
- 11. Replace the computer cover.

CONGRATULATIONS! You have just installed the ZIP CHIP. You may now proceed to the chapter on USE OF THE ZIP CHIP.



Installing the ZIP CHIP in an Apple //c - Installing the ZIP CHIP involves three processes. One, opening the Apple //c, two, installing the ZIP CHIP and three, closing the Apple //c. All of these are simple step-by-step processes. It is recognized that most Apple //c owners have never opened their computers and may wish to have the chip installed by a local Apple Dealer. While that may be done it is not necessary as the installation is quite simple. The only tool required other than the supplied Chip Removal Tool is a small Phillips screwdriver and a little patience.

<u>Opening the Apple //c</u> - Follow this process carefully step-by-step and you should have no trouble opening the Apple //c.

- 1. Turn power off to the computer, and remove all wires and cables going to it. Remove any disk that may be in the drive.
- 2. Turn the computer upside down and unscrew the two screws (marked 'A' in the illustration) at the keyboard end corners.
- 3. Unscrew the two recessed screws up the side from the corners, (marked B in the illustration.) Turn the computer right side up to drop these screws free.
- 4. At the back of the computer where the handle connects to the case there are two screws, (marked 'C' in the illustration.) Unscrew both of these.
- 5. Turn the computer right side up with the keyboard facing you.
- 6. Slide the short end of the Chip Removal Tool into the crack between the two halves of the case at approximately the space bar point on the case.
- 7. Gently rock the tool up until the case lock pops free.
- Lift up on the top half of the case and it will pop free of the computer.
- 9. Gently lift the keyboard and lay it upside down on top of the disk drive.

Now we are ready to install the ZIP CHIP

Installing the ZIP CHIP

10. Locate the 6502 or 65C02 CPU chip. It is the long chip to the right of the speaker on the front of the motherboard. It is the longer of the two chips in sockets; between rows 18 and 19 on column E.

NOTE: Some models of the Apple //c have a keyboard different from that shown in the illustration and some will have the IOU and MMU chips in sockets.

Those with Apple //c computers that have special memory boards or CP/M boards installed may have to search for the CPU chip. The markings on the chip should read:

©NCR 65C02A 609-0380113 C817801 8530A

or something similar to this. DO NOT REMOVE ANY CHIP UNTIL YOU ARE SURE.

- 11. The front of the CPU chip is to the left, facing the speaker volume control side of the computer.
- 12. Slide the short end of the Chip Removal Tool in the slot between the CPU chip and the socket.
- 13. Gently rock the tool lifting the chip from the socket.
- 14. Do the same to the other end of the chip.
- 15. Grasp the CPU chip and remove it from the computer. Put it in a safe place.
- 16. Take the ZIP CHIP and hold it so that the notched end faces left.
- 17. Lower the **ZIP CHIP** to the socket. Press the chip gently into the socket. Make sure that all the pins are going into holes in the socket.
- 18. When the chip is in place, firmly press down on each end to "seat" the chip.

## Now to close the Apple //c.

# Closing the Apple //c

- 19. Gently pick up the keyboard and turn it right side up. Lower the keyboard in place. The metal tab on the back end of the keyboard fits into a slot in the side of the disk drive.
- 20. Two models of the Apple //c case top are known. One has the back attached to the case top, the other has the back separate. In either case the top is first hooked on the back and rocked forward and down over the top of the computer.

- 21. Those cases with back separate must be carefully assembled to be sure that the back is in proper place as the top is installed.
- 22. Press down firmly on the case top just in front of the space bar. The case should snap together. Press all around the front and sides of the case to "seat" the case top.
- 23. Turn the computer upside down and replace the screws. NOTE: The recessed screws (B) are different from the other four. Take care <u>not to overtighten</u> the screws.

**CONGRATULATIONS!** You have just installed the **ZIP** CHIP. You may now proceed to the chapter on **USE** OF THE ZIP CHIP.

# **USE OF ZIP CHIP**

# To Run At ZIP CHIP System Speed

For most applications, the **ZIP CHIP** can be used as installed. The default settings are:

To use your **ZIP CHIP**, simply turn your computer on. After a minor hesitation and a high pitched beep, your boot program will start. Pressing the keys CTRL - OPEN APPLE - RESET on Apple / /e and //c will also startup.

**NOTE:** When doing a startup with the CTRL - OPEN APPLE - RESET, Hold the OPEN APPLE key down until a beep is heard from the speaker. (Approx. 2 seconds.)

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Warning:

Do **not** press the SPACE bar while doing a startup. The SPACE bar option is only used for non-standard startup as described in the section on Configuration.

## To Run At Normal Apple Speed

On startup, press the ESCape key to run the **ZIP** CHIP at normal Apple speed (1 megahertz). This is for use with hardware such as CP/M boards, or for software that is unusable at high speed such as some arcade type games. The key must be pressed within the count of two. The speaker sound and the system speed will be normal (1 megahertz.)

Startup can be either POWER ON or by pressing the CTRL - OPEN APPLE - RESET keys. **NOTE:** When using the CTRL - OPEN APPLE - RESET for startup, hold the OPEN APPLE key down, (even if you press the ESCape key also,) until a beep is heard from the speaker, (approx. 2 seconds.) Once the **ZIP CHIP** is set to normal speed, it cannot be reset to high speed until the next startup or by custom programs.

## ZIP CHIP UTILITY PROGRAMS

With your **ZIP CHIP** there is a free disk containing highly useful programs. Side one of the disk contains PRODOS versions, side two contains DOS 3.3 versions. These programs are:

**ZIP.CONFIG** used to configure the **ZIP CHIP** and allow the user to set each slot to the desired speed.

**ZIP.DIAGS** used to examine in detail the operation of the **ZIP** CHIP.

**ZIP.SYS.CHK** used to preform a comprehensive memory test of your Apple // while also checking the performance of your **ZIP CHIP**.

**ZIP.HELLO** used to boot your Apple DOS 3.3 disks in any configuration you wish (DOS 3.3 side only).

**ZIP.STARTUP** used to boot your Apple PRODOS disks in any configuration you wish. This program is located on side two (PRODOS side) of the supplied disk.

This manual is reproduced in a text file on the disk along with a read/print program, **ZIP.INSTRUCT**. All programs (except **ZIP.HELLO** and **ZIP.STARTUP**,) are duplicated on both the DOS 3.3 and the PRODOS sides of the disk.

When you boot up either the PRODOS side or the DOS 3.3 side of the disk the following menu should appear:

MAIN MENU	ZIPCHIP II	1.00	
	CONFIGURE INSTALLED		
B) C) D}	RUN ZIP DIAGNOSTICS RUN ZIP SYSTEM CHECK RUN ZIP CONFIGURER RUN ZIP INSTRUCTIONS EXIT MENU		

# WHICH?

<u>ZIP CHIP Diagnostic Program</u> - Selecting 'A' will display the diagnostic program menu/results screen. From this menu each function of the **ZIP CHIP** can be tested along with all or selected parts of the RAM cache. Any failures will be displayed on this screen. To exit the diagnostic, perform a startup.

<u>System Diagnostic Program</u> - Selecting 'B' will display the diagnostic program menu/results screen. Any or all of the displayed Apple functions can be tested and the results will display on this screen. To exit the diagnostic, perform a startup.

<u>ZIP CHIP Configure Program</u> - Selecting 'C' causes the following Configuration Menu to display:

A)	ZIPCHIP		ON
B)	ZIPCHIP SP	PEED	4.0000 MHZ
C)	LANGUAGE	CARD	CACHED
D)	PADDLE SP	PEED	NORMAL
E)	SPEAKER S	SPEED	FAST
F)	SLOT 1	SPEED	FAST
G)	SLOT 2	SPEED	NORMAL
H)	SLOT 3	SPEED	FAST
I)	SLOT 4	SPEED	FAST
J)	SLOT 5	SPEED	NORMAL
K)	SLOT 6	SPEED	NORMAL
L)	SLOT 7	SPEED	NORMAL

CONFIGURER ZIPCHIP II-4 1.00

X) EXIT CONFIGURER

# OPTION?

Selecting 'D' through 'L' will cause the speed to toggle from FAST to NORMAL or NORMAL to FAST.

WARNING: If you have an Apple Floppy Disk Drive in Slot 6, changing the speed to FAST may cause damage to the data on the disk.

Selecting 'A' will cause the message to toggle from ON to OFF and the system will run at normal Apple speed. Selecting 'B' will cause one of twenty possible system speeds to display. The display will step through a speed each time that 'B' is selected. Selecting 'C' will cause the display to toggle from CACHED to NOT CACHED. NOT CACHED is used only when you have bank switched memory cards in slots other than the Apple auxiliary slot. When you select X, a message will display at the bottom of the screen:

## SAVE CONFIGURATION (ESC TO RESUME)?

Press the Escape key to continue with configuration or type Y to create the file ZIPCFG on the disk and exit the Configuration Program. Pressing any other key other than a Y or the Escape key will set the configuration selected but will <u>not</u> create the file **ZIPCFG**. A configure once set will remain in effect until the next power off or CTRL - OPEN APPLE - RESET.

NOTE: Once a configure is done, the words:

## CONFIGURE INSTALLED

(Shown in italics on the sample Main Menu), will display on the Main Menu the next time startup is done on this disk.

Once a Configure is done the file **ZIPCFG** is created on the disk. If this file, together with the file **ZIP.STARTUP** (for PRODOS) or **ZIP.HELLO** (for DOS 3.3), is transferred to another disk, that disk will boot with the configuration you have set. Once transferred, files **ZIP.STARTUP** or **ZIP.HELLO** should be renamed **STARTUP** or **HELLO**.

Starting up Non-standard DOS Disks - Once a Configure has been set, non-standard DOS disks can be booted by a **PR#6**, or any slot you wish. A configure will be set any time a disk containing **ZIPCFG** and one of the supplied booting programs is used.

The startup sequence CTRL - OPEN APPLE - RESET can also be used providing the SPACE bar is pressed immediately following the RESET key. The OPEN APPLE key must be pressed and held (even if the SPACE bar is pressed,) until a beep is heard from the speaker.) The **ZIP CHIP** options set with Configure will remain in effect, but a new copy of **ZIPCFG** will not be written to disk.

## CAUTION

The following information is for programmers only. Only those familiar with assembly language and the software structure of the Apple // should attempt to modify the **ZIP CHIP** or add the features to their code. All others beware...there is deep water ahead.

#### ZIP CHIP TECHNICAL INFORMATION

**ZIP CHIP** Theory of Operation.- The Zip Technology **ZIP CHIP** uses a patented method of micro-computer speed-up based on caching. A small cache of RAM inside the **ZIP CHIP** can be read from and written to at speeds up to and including 4 megahertz. This RAM is totally transparent to the user and it cannot be accessed by software because it has no prearranged address start. Data within this RAM can come from anywhere in the Apple's main memory, language card memory, ROM or from an Auxiliary memory card.

Caching as used in **ZIP CHIP** works as follows: First a data read is initiated by the processor, (the 65C02 within the **ZIP CHIP**). Then **ZIP CHIP** looks at it's TAG cache to see if the data is in it's DATA cache. If it is not, **ZIP CHIP** slows down to normal Apple speed (1 megahertz), locates and reads the data simultaneously depositing it in the DATA cache. A TAG value is then placed into TAG cache for future reference. If the data is found in cache **ZIP CHIP** accesses it at system speed (.666 to 4.0 megahertz) and processes it. Once data is in cache, Apple memory is NOT accessed in any way. Further processing occurs within the chip at the set speed. Writes to memory always update TAG, DATA and Apple memory.

Up to 30 banks of RAMWORKS style auxiliary memory can be cached. (2 megabytes) All other memory can be accessed but at normal Apple speed.

A tap of the Apple Phase 0 clock, (a 1 millisecond pulse,) is available. A synchronous sequence consists of setting the system speed to normal Apple speed (1.0204 megahertz) for a specific time period.

While this is not a comprehensive explanation of the internal functioning of **ZIP CHIP**, it should be sufficient for programmers to access and use the various features.

### Table 1 - Internal Structure of the ZIP CHIP

The following is inside the ZIP CHIP

- o 65C02 Processor Chip (rated to 4.0 megahertz)
- o ZIP CHIP Gate Array circuitry
- o 8k TAG Cache
- o 8k DATA Cache
- o 16.00 megahertz Clock

Control of the **ZIP CHIP** from software is through softswitch registers inside the chip. Extreme care must be used when changing the contents of these registers because improper use can render a **ZIP CHIP** startup floppy disk functionally unusable.

Each register may perform a number of related or unrelated functions. Table 2 shows the **ZIP CHIP** registers, how they are accessed and what each bit of the register does. An in-depth discussion of each register follows this table.

	Tabl	e 2 - ZIP CHII	PREGIST	ERS	
Register	How				
Address	Accessed	Bit/Functio	n		
\$C05A	Write	\$A5 Locks	the ZIP CI	HIP.	
		4 consecut	ive \$5A wr	tes unlock ZI	P CHIP.
		While unlo	cked, any	write other that	an \$A5 or
				lefinate syncro	
		sequence.			
\$C05B	Write	Any hex byte written will enable ZIP CHIP.			
\$C05B	Read	Reads the current status of the following:			owing:
		bit 0 & 1 - I	Ramsize w	here:	
		RAMSIZ	E1 RAMS	IZE0 SIZE	
		0	0	8K	
		0	1	16K	
		1	0	32K	
		1	1	64K	

Register	How		
Address	Accessed	Bit/Function	
		bit 2 - unused	-
		bit 3 - Delay (for memory)	
		0 = Fast Mode - Delay not	
		in effect	
		1 = Sync Mode - Delay in	
		effect	
		bit 4 - Disabled/enabled	
		0 = Chip Enabled	
		1 = Chip Disabled	
		bit 5 - Paddle fast/normal	
		0 = Fast Mode	
		1 = Synchronous Mode (Normal)	
		bit 6 - Cache Updated by data read	
		0 = No update	
		1 = Yes cache updated	
		bit 7 - Clock Pulse - 1.0035 milliseconds	
		Edges occur at .50175 milliseconds	
\$C05C	Read/Write	Slot/Speaker set and read	
		0 = Set slot/speaker Fast	
		1 = Set slot/speaker Normal	
		bit 0 - Speaker bit 4 - Slot 4	
		bit 1 - Slot 1 bit 5 - Slot 5	
		bit 2 - Slot 2 bit 6 - Slot 6	
		bit 3 - Slot 3 bit 7 - Slot 7	
\$C05D	Write	Set System Speed	
		bit 0 - unused bit 4 - Clk4/5	
		bit 1 - unused bit 5 - Clk5/6	
		bit 3 - Clk3/4 bit 7 - Clk/4	
		bit 2 - Clk2/3 bit 6 - Clk/2	

Register       How         Address       Accessed       Bit/Function         SC05E       Write       Enable/Disable Synchronous Operation for I/C         Devices       bit 0 through bit 6 - Not Used       bit 7 - Enable/Disable Delay         0 = Enable/Disable Delay       0 = Enable/Disable Delay         1 = Disable and Reset Delay       1 = Disable and Reset Delay         6C05E       Read       Read Apple softswitches         0 = False       1 = True       bit 0 - ROMRD       bit 4 - 80STORE         bit 1 - RAMBNK       bit 5 - MWR*       bit 2 - PAGE2       bit 6 - MRD*         bit 3 - HIRES       bit 7 - ALTZP         GC05F       Write       Paddle Speed, Bank Switch Language Card         bit 0 through bit 5 - Not Used       bit 6 - Paddle Set       0 = Disable Paddle Delay
SC05E       Write       Enable/Disable Synchronous Operation for I/C         Devices       bit 0 through bit 6 - Not Used         bit 7 - Enable/Disable Delay       0 = Enable Delay         0 = Enable Delay       1 = Disable and Reset Delay         1 = Disable and Reset Delay       1 = True         bit 0 - ROMRD       bit 4 - 80STORE         bit 1 - RAMBNK       bit 5 - MWR*         bit 2 - PAGE2       bit 6 - MRD*         bit 3 - HIRES       bit 7 - ALTZP         SC05F       Write       Paddle Speed, Bank Switch Language Card         bit 0 through bit 5 - Not Used       bit 6 - Paddle Set         0 = Disable Paddle Delay       0 = Disable Paddle Delay
Devices         bit 0 through bit 6 - Not Used         bit 7 - Enable/Disable Delay         0 = Enable Delay         1 = Disable and Reset Delay         1 = Disable and Reset Delay         0 = False         0 = False         1 = True         bit 0 - ROMRD       bit 4 - 80STORE         bit 1 - RAMBNK       bit 5 - MWR*         bit 2 - PAGE2       bit 6 - MRD*         bit 3 - HIRES       bit 7 - ALTZP         SC05F       Write       Paddle Speed, Bank Switch Language Card         bit 0 through bit 5 - Not Used       bit 6 - Paddle Set         0 = Disable Paddle Delay       0 = Disable Paddle Delay
bit 7 - Enable/Disable Delay 0 = Enable Delay 1 = Disable and Reset Delay 3 = Disable and Reset Delay 6 = False 1 = True bit 0 - ROMRD bit 4 - 80STORE bit 1 - RAMBNK bit 5 - MWR* bit 2 - PAGE2 bit 6 - MRD* bit 3 - HIRES bit 7 - ALTZP 6 C05F Write Paddle Speed, Bank Switch Language Card bit 0 through bit 5 - Not Used bit 6 - Paddle Set 0 = Disable Paddle Delay
bit 7 - Enable/Disable Delay 0 = Enable Delay 1 = Disable and Reset Delay 3 = Disable and Reset Delay 6 = False 1 = True bit 0 - ROMRD bit 4 - 80STORE bit 1 - RAMBNK bit 5 - MWR* bit 2 - PAGE2 bit 6 - MRD* bit 3 - HIRES bit 7 - ALTZP 6 C05F Write Paddle Speed, Bank Switch Language Card bit 0 through bit 5 - Not Used bit 6 - Paddle Set 0 = Disable Paddle Delay
0 = Enable Delay         1 = Disable and Reset Delay         3C05E       Read         Read Apple softswitches         0 = False         1 = True         bit 0 - ROMRD       bit 4 - 80STORE         bit 1 - RAMBNK       bit 5 - MWR*         bit 2 - PAGE2       bit 6 - MRD*         bit 3 - HIRES       bit 7 - ALTZP         3C05F       Write       Paddle Speed, Bank Switch Language Card         bit 0 through bit 5 - Not Used       bit 6 - Paddle Set         0 = Disable Paddle Delay       0 = Disable Paddle Delay
1 = Disable and Reset Delay         3C05E       Read         Read Apple softswitches         0 = False         1 = True         bit 0 - ROMRD       bit 4 - 80STORE         bit 1 - RAMBNK       bit 5 - MWR*         bit 2 - PAGE2       bit 6 - MRD*         bit 3 - HIRES       bit 7 - ALTZP         3C05F       Write       Paddle Speed, Bank Switch Language Card         bit 0 through bit 5 - Not Used       bit 6 - Paddle Set         0 = Disable Paddle Delay       0 = Disable Paddle Delay
0 = False         1 = True         bit 0 - ROMRD       bit 4 - 80STORE         bit 1 - RAMBNK       bit 5 - MWR*         bit 2 - PAGE2       bit 6 - MRD*         bit 3 - HIRES       bit 7 - ALTZP         SC05F       Write       Paddle Speed, Bank Switch Language Card         bit 0 through bit 5 - Not Used       bit 6 - Paddle Set         0 = Disable Paddle Delay
1 = True         bit 0 - ROMRD       bit 4 - 80STORE         bit 1 - RAMBNK       bit 5 - MWR*         bit 2 - PAGE2       bit 6 - MRD*         bit 3 - HIRES       bit 7 - ALTZP         C05F       Write       Paddle Speed, Bank Switch Language Card         bit 0 through bit 5 - Not Used       bit 6 - Paddle Set         0 = Disable Paddle Delay
bit 0 - ROMRD bit 4 - 80STORE bit 1 - RAMBNK bit 5 - MWR* bit 2 - PAGE2 bit 6 - MRD* bit 3 - HIRES bit 7 - ALTZP SC05F Write Paddle Speed, Bank Switch Language Card bit 0 through bit 5 - Not Used bit 6 - Paddle Set 0 = Disable Paddle Delay
bit 1 - RAMBNK bit 5 - MWR* bit 2 - PAGE2 bit 6 - MRD* bit 3 - HIRES bit 7 - ALTZP COSF Write Paddle Speed, Bank Switch Language Card bit 0 through bit 5 - Not Used bit 6 - Paddle Set 0 = Disable Paddle Delay
bit 2 - PAGE2       bit 6 - MRD*         bit 3 - HIRES       bit 7 - ALTZP         C05F       Write       Paddle Speed, Bank Switch Language Card         bit 0 through bit 5 - Not Used       bit 6 - Paddle Set         0 = Disable Paddle Delay
C05F Write Paddle Speed, Bank Switch Language Card bit 0 through bit 5 - Not Used bit 6 - Paddle Set 0 = Disable Paddle Delay
C05F Write Paddle Speed, Bank Switch Language Card bit 0 through bit 5 - Not Used bit 6 - Paddle Set 0 = Disable Paddle Delay
bit 0 through bit 5 - Not Used bit 6 - Paddle Set 0 = Disable Paddle Delay
bit 6 - Paddle Set 0 = Disable Paddle Delay
0 = Disable Paddle Delay
1 = Enable Paddle Delay
bit 7 - Language Card Enable/Disable
0 = Enable Cache of Language Card Memory
1 = Disable Cache of Language Card Memory

### ZIP CHIP REGISTERS DESCRIPTION

<u>\$C05A SOFTSWITCH REGISTER.</u> **ZIP CHIP** softswitch \$C05A allows access to all other **ZIP CHIP** registers. This is done through the Lock/Unlock feature.

To lock the **ZIP CHIP** registers write a \$A5 to address \$C05A. Unlocking **ZIP CHIP** is a little more difficult. To prevent accidental unlocking by programs, at least four writes of \$5A in succession must be done. Any other program write instruction coming between the first four \$5A writes will invalidate the unlock. More than four \$5A writes are ignored by the softswitch. Recommended assembler code to unlock **ZIP CHIP** is:

LDA	#\$5A
STA	\$C05A

While the **ZIP CHIP** is unlocked, any value other than a \$5A or a \$A5 will cause an indefinite Synchronous Sequence, (turns off the High Speed Mode) setting the system to normal Apple speed of 1.0204 megahertz.

<u>\$C05B SOFTSWITCH REGISTER</u> - This softswitch is used for a variety of functions. Primarily it is used to turn on the **ZIP CHIP** to high speed. This is done by any write to \$C05B while the **ZIP CHIP** is unlocked. Reads of this softswitch obtain data on a variety of **ZIP CHIP** functions. Of particular interest to those needing a precise timing signal, is the one (1.0035) millisecond clock pulse at bit seven of this register. The bits of this register are used as follows:

Bit 0 and bit 1 show the size of cache memory.

Bit two is unused.

Bit three is a one if the delay circuitry is active. A slot delay begins when an access is done to the I/O memory area of a slot set for Synchronous Sequence (\$C0nX - where 'n' is the slot number plus 8 and 'X' is a number from \$0 to \$F) The access begins a 52 to 54 millisecond period during which all Reads come from the Apple to keep the computer at Normal speed. (1.0204 megahertz) When the paddle or the speaker is set for synchronous sequence, a softswitch access results in a delay of 5 milliseconds. A zero in bit three indicates that no delay is in effect. When bit four is a one, it shows that the **ZIP CHIP** cannot cache code. This bit will be set if the user presses the ESCape key during boot or if a byte other than \$A5 or \$5A is entered into register \$C05A while the **ZIP CHIP** is unlocked. A zero in bit four indicates that caching is enabled and the **ZIP CHIP** can run at set system speed.

Bit five indicates whether or not a paddle softswitch access will cause a synchronous sequence. If the bit is a zero, then an access to \$C070 will be at system speed. If the bit is a one, then a 5 millisecond synchronous sequence will occur before returning to system speed.

Bit six confirms that a data read has updated the cache memory. A one indicates that cache has been updated; a zero indicates that it has not.

Bit seven is a tap on the Apple Phase 0 clock divided by 1024. This bit oscillates at a one (1.0035)millisecond rate. The pulse edges occur at .50175 millisecond intervals. This signal can be used for precise timing applications.

<u>\$C05C SOFTSWITCH REGISTER</u> - The softswitch register at \$C05C indicates and determines which slots will run at the speed set in **ZIP CHIP** or at normal Apple speed. The speaker is also controlled from this register. Reads of this register show the current condition of the speaker and slots.

To enable a slot (or the speaker) to run a synchronous sequence, a one is written to the appropriate bit. Bit 0 controls the speaker. Bits 1 through bit 7 control slots 1 through 7 respectively. A one written to bit 0 will allow a five millisecond synchronous sequence for softswitch access of \$C030.

**CAUTION:** If an I/O device such as the Apple Floppy Disk Drive is in a slot defined for other than normal access, disks in that drive may be rendered unreadable. Be sure that a device can safely run at speeds above normal Apple speed before setting its slot to a higher speed.

<u>\$C05D SOFTSWITCH REGISTER</u> - The \$C05D softswitch register can set the system speed to one of twenty speeds from 0.6666 megahertz to

4.0000 megahertz. The following table shows the bit patterns for bits 2 through 7 as used to select one of the eighteen available clock speeds. An 'X' in the pattern indicates that this bit is ignored by the register for this speed. (i.e. 'X' = Don't care.)

NOTE: These speeds are for cache reads and writes only. Apple accesses will still be at normal Apple speed. If a program can run totally within cache memory, then the above speeds are accurate. If the program is larger than cache, then the actual system speed will be different from those noted.

	Table 3 - \$C05D Bit Patterns			
Bit	76543210	Speed (in MHZ)		
	0 0 0 0 0 0.X.X	4.0000		
	00001.X.X	2.6667		
	00001X.X.X	3.0000		
	0001XX.X.X	3.2000		
	0 0 1 X X X.X.X	3.3333		
	01000.X.X	2.0000		
	010001.X.X	1.3333		
	01001X.X.X	1.5000		
	0101XX.X.X	1.6000		
	0 1 1 X X X.X.X	1.6667		
	100001.X.X	0.6667		
	10001X.X.X	0.7500		
	1 0 0 1 X X.X.X	0.8000		
	1 0 1 X X X.X.X	0.8333		
	11000.X.X	1.3333		
	110001.X.X	0.8889		
	11001X.X.X	1.0000		
	1101XX.X.X	1.0667		
	1 1 1 X X X.X.X	1.1111		

<u>\$C05E SOFTSWITCH REGISTER</u> - The \$C05E softswitch register has greatly different functions between Read and Write. A \$C05E read is similar to a simultaneous read of eight softswitches, (for determining whether the Apple is in AltZP or MainZP, etc.) See table 2 for the exact switches tested. Only bit 7 of \$C05E is functional in a write. Bit 7 is the delay switch controlling Synchronous Sequences. If this is a zero, then Synchronous Sequences are enabled. If this bit is set to one while a delay is active, then the delay is terminated immediately and Synchronous Sequences are disabled. Control of this register can ensure that a piece of code will run at set system speed.

<u>\$C05F SOFTSWITCH REGISTER</u> -This register controls compatibility with bank switched memory cards and determines if Paddle accesses cause Synchronous Sequences. The two active bits in this register control the caching of language card memory.and the slowing of the system for paddle use Bit 7 (normally zero) when set to one disables caching of language card memory. This will allow large memory cards to run with **ZIP CHIP**. Bit 6 controls paddle softswitch access. When set to one, accesses to \$C070 cause a 5 millisecond synchronous sequence. When set to zero, accesses to \$C070 cause no Synchronous Sequence.

### **PROGRAMMING HINTS**

Programmers are encouraged to work the features of **ZIP CHIP** into their code. To assist in this the following samples are provided.

NOTE: \$C05A to C05D are Annunciators. \$C05E and \$C05F are Double HIRES

When **ZIP CHIP** registers are accessed with **ZIP CHIP** unlocked, the Annunciators and Double HIRES switches are <u>not</u> affected provided that the code accessing the **ZIP CHIP** registers is executing entirely from cache. When unlocking the **ZIP CHIP**, the first four writes to \$C05A <u>do affect</u> Annunciator 2. Any devices using Annunciator 2 may also be affected.

The following code accesses **ZIP CHIP** registers completely from cache. This outline is recommended for opening and altering the **ZIP CHIP** softswitch registers:

	LDY	#\$5A	Open value
	STY	\$C05A	Open the ZIP CHIP
	STY	\$C05A	· · · · · · · · · · · · · · · · · · ·
	STY	\$C05A	
	STY	\$C05A	
	LDY	\$C05B	Is ZIP CHIP enabled?
	STY	\$C05B	Always enable ZIP CHIP
			(Any value here will suffice)
LDX	#\$00	256 bytes	(if altering code <257 bytes)
CACHE	LDA	ALTER,X	Cache the altering code
	INX		
	BNE	CACHE	
ALTER	NOP		Your own code goes here

Use the following code to verify that **ZIP CHIP** is installed in a particular system. Remember to unlock the chip first.

ALTER	LDA \$C05C EOR #\$FF STA \$C05C CMP \$C05C BNE NOZIP	Get the slot delay status Flip it Save it Correct? No, ZIP CHIP not found.
	EOR #\$FF STA \$C05C CMP \$C05C BNE NOZIP	Get back old status Save it Correct? No, ZIP CHIP not found.
GOTAZIP NOZIP	NOP NOP	Yes, ZIP CHIP found! No ZIP CHIP found.

If the code gets to GOTAZIP, then you are certain that the computer has a **ZIP CHIP** installed.

# A FINAL NOTE

**Zip** Technology maintains a Technical Service Hotline to assist users and software developers with the **ZIP** CHIP. Direct all inquires to:

# ZIP TECHNOLOGY 11340 W. OLYMPIC BLVD. LOS ANGELES, CA 90064

or call our Hotline (213) 473-8350 between the hours of 9:00 AM to 5:00 PM Pacific time.

**Zip** Technology currently has established a 24 hour dial-up message and product ordering bulletin board for our customers convenience. The telephone number is (213) 433-8694. The board operates at either 300, 1200 or 2400 baud, depending upon the speed of the caller. Watch our ads for more on this exciting new service.

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